# Syllabus

Course Program

# Circuitry Design

**Specialty**
141 – Electric power engineering, electrical engineering and electromechanics

**Institute**
Educational and Scientific Institute of Energy, Electronics and Electromechanics

**Educational program**
Electric drive, Mechatronics and Robotics

**Department**
Department of Automated Electromechanics Systems (129)

**Level of education**
Bachelor's level.

**Course type**
Special (professional),

**Semester**
5

**Language of instruction**
English,

## Lecturers and course developers

**Yaroslav Kyrylenko**

Yaroslav.Kyrylenko@ieee.khpi.edu.ua
Assistant at Department of Automated Electromechanics Systems of NTU "KhPI".

Author and co-author of more than 9 scientific publications.
Courses: "Embedded control systems in mechatronics", "Programming in the C language", "Вбудовані системи керування в мехатроніці", Industrial Robots, Digital circuits.
More about the lecturer on the department's website

## General information

### Summary

Introduction to modern digital logic design, combinational logic, switch logic and basic gates, Boolean algebra, two-level logic, regular logic structures, multi-level networks and transformations, programmable logic devices, time response. Sequential logic, networks with feedback, basic latches and flip-flops, timing methodologies, registers and counters, programmable logic devices. Finite state machine design, concepts of FSMs, basic design approach, specification methods, state minimization, state encoding, FSM partitioning, implementation of FSMs, programmable logic devices. Elements of computers, arithmetic circuits, arithmetic and logic units, register and bus structures, controllers/ sequencers, microprogramming. Experience with computer-aided design tools for logic design, schematic entry, state diagram entry, hardware description language entry, compilation to logic networks, simulation, mapping to programmable logic devices. Practical topics, non-gate logic, asynchronous inputs and metastability, memories: RAM and ROM, Implementation technologies and mapping problems expressed in words to digital abstractions.

## Course objectives and goals

1) Convert signed/unsigned, integer/fixed-point decimal numbers to/from binary/hex representations; perform integer/fixed-point addition/subtraction using binary/hex number representations; and define precision and overflow for integer/fixed-point, signed/unsigned, addition/subtraction operations.
2) Define basic (AND, OR, NOT) and derived (e.g., NAND, NOR, XOR) Boolean operations; enumerate Boolean algebra laws and theorems; use basic and derived Boolean operations to evaluate Boolean expressions; and write and simplify Boolean expressions by applying appropriate laws and theorems and other techniques (e.g., Karnaugh maps).
3) Describe electrical representations of TRUE/FALSE; describe the high-impedance condition and logic gate implementation such as a tri-state buffer; and discuss the physical properties of logic gates such as fan-in, fan-out, propagation delay, power consumption, logic voltage levels, and noise margin and their impact on the constraints and tradeoffs of a design.
4) Implement Boolean expressions using the two-level gate forms of AND-OR, OR-AND, NAND-NAND, NOR-NOR and positive/negative conventions; and using multiple gating levels and positive/negative conventions.
5) Describe and design single-bit/multi-bit structure/operation of combinational building blocks such as multiplexers, demultiplexers, decoders, and encoders; describe and design the structure/operation of arithmetic building blocks such adders (ripple-carry), subtractor, shifters, and comparators; describe and design structures for improving adder performance such as carry lookahead and carry select; and analyze and design combinational circuits (e.g., arithmetic logic unit, ALU) in a hierarchical, modular manner, using standard and custom combinational building blocks.
6) Define a clock signal using period, frequency, and duty-cycle parameters; describe propagation delay, setup time, and hold time for basic latches and flip-flops; and analyze and create timing diagrams for sequential block operation.
7) Explain the structure/operation of basic latches (D, SR) and flip-flops (D, JK, T); describe and design the structure/operation of sequential building blocks such as registers, counters, and shift registers; enumerate design tradeoffs in using different types of basic storage elements for sequential building block implementation.
8) Describe the characteristics of static memory types such as static random-access memory (SRAM), and ROM.
9) Define important engineering constraints such as timing, performance, power, size, weight, cost, and their tradeoffs in the context of digital systems design.
10) Use a contemporary analysis/design/simulation software/hardware toolchain to prototype in hardware various digital logic circuits entailing combinational and sequential circuits.

## Format of classes

Lectures, laboratory classes, consultations, self-study. Final control in the form of an exam.

## Competencies

"Physics", "Electric machines and devices", "Industrial electronics", "Fundamentals of microprocessor technology"

## Learning outcomes

After studying this course, the students would gain enough knowledge
1. Have a thorough understanding of the fundamental concepts and techniques used in digital electronics.
2. To understand and examine the structure of various number systems and its application in digital design.
3. The ability to understand, analyze and design various combinational and sequential circuits.
4. Ability to identify basic requirements for a design application and propose a cost effective solution.
5. The ability to identify and prevent various hazards and timing problems in a digital design.
6. To develop skill to build, and troubleshoot digital circuits.

## Student workload

The total volume of the course is 120 hours (4 ECTS credits): lectures - 32 hours, laboratory classes - 16 hours, practical studies - ,self-study - 56 hours.

### Course prerequisites

None

### Features of the course, teaching and learning methods, and technologies

Learn the basics of simulating analog electric circuits in Simscape. Use the physical network approach to simulate electrical filters and faulty power supplies, and analyze their performance in the time and frequency domains.

## Program of the course

### Topics of the lectures

Topic 1. Electric Circuit Theory Review
Topic 2. Digital and Analog, Number Systems
Topic 3. Digital Signals, Serial and Parallel Transmission, AND, OR, NOT gates, ICs
Topic 4. Combinational Logic, Boolean Laws and Algebra, DeMorgan's Theorem
Topic 5. NAND/NOR Universality, POS, SOP, K-maps
Topic 6. XOR, XNOR, Parity Circuits, Controlled Inverters
Topic 7. Binary Addition and Subtraction, Two's Complement System and Arithmetic, BCD Arithmetic, Half and Full Adders, Adder ICs, Adder/Subtractor, ALU
Topic 8. Comparators, Decoding/Encoding, Code Converters, MUXs, DeMUXs, Analog MUX/DeMUX, System Design
Topic 9. Sequential Logic; Registers; SR Latch; D, JK, T Flip Flops; MS and Edge Triggering; IC Flip Flops; Octal FF chip; FF Function Tables
Topic 10. Sequential Circuit Analysis, Ripple Counters, Modulus, Divide-by-n Counters, Synchronous Counters
Topic 11. Relays, Diodes, Transistor as a Switch, TTL and CMOS, DIP and SMD
Topic 12. TTL Family, Totem Pole and Open Collector Outputs, CMOS Family, Interfacing Logic Families, Auto Delay Gate, Auto Reset Circuit, Schmitt Trigger, Debouncing, Pull-up Resistors,

### Topics of the workshops

No lectures classes in this course

### Topics of the laboratory classes

Topic 1. Electric Circuit Theory Review
Topic 2. Digital and Analog, Number Systems
Topic 3. Digital Signals, Serial and Parallel Transmission, AND, OR, NOT gates, ICs
Topic 4. Combinational Logic, Boolean Laws and Algebra, DeMorgan's Theorem
Topic 5. NAND/NOR Universality, POS, SOP, K-maps
Topic 6. XOR, XNOR, Parity Circuits, Controlled Inverters
Topic 7. Binary Addition and Subtraction, Two's Complement System and Arithmetic, BCD Arithmetic, Half and Full Adders, Adder ICs, Adder/Subtractor, ALU
Topic 8. Comparators, Decoding/Encoding, Code Converters, MUXs, DeMUXs, Analog MUX/DeMUX, System Design
Topic 9. Sequential Logic; Registers; SR Latch; D, JK, T Flip Flops; MS and Edge Triggering; IC Flip Flops; Octal FF chip; FF Function Tables
Topic 10. Sequential Circuit Analysis, Ripple Counters, Modulus, Divide-by-n Counters, Synchronous Counters
Topic 11. Relays, Diodes, Transistor as a Switch, TTL and CMOS, DIP and SMD
Topic 12. TTL Family, Totem Pole and Open Collector Outputs, CMOS Family, Interfacing Logic Families, Auto Delay Gate, Auto Reset Circuit, Schmitt Trigger, Debouncing, Pull-up Resistors,

### Self-study

Information on self-study and individual assignments (reports, course projects, etc.), if it is necessary according to the plan. Also, methods of control and assessment of self-study.

## Course materials and recommended reading

1. Sarah Harris and David Harris. 2015. Digital Design and Computer Architecture: ARM Edition (1st. ed.). Morgan Kaufmann Publishers Inc., San Francisco, CA, USA.

## Assessment and grading

### Criteria for assessment of student performance, and the final score structure

The final grade consists of the results of the evaluation of final exam (50%) and laboratory reports (50%)

### Grading scale

| Total points | National | ECTS |
|---|---|---|
| 90–100 | Excellent | A |
| 82–89 | Good | B |
| 75–81 | Good | C |
| 64–74 | Satisfactory | D |
| 60–63 | Satisfactory | E |
| 35–59 | Unsatisfactory (requires additional learning) | FX |
| 1–34 | Unsatisfactory (requires repetition of the course) | F |

## Norms of academic integrity and course policy

The student must adhere to the Code of Ethics of Academic Relations and Integrity of NTU "KhPI": to demonstrate discipline, good manners, kindness, honesty, and responsibility. Conflict situations should be openly discussed in academic groups with a lecturer, and if it is impossible to resolve the conflict, they should be brought to the attention of the Institute's management.
Regulatory and legal documents related to the implementation of the principles of academic integrity at NTU "KhPI" are available on the website: http://blogs.kpi.kharkov.ua/v2/nv/akademichna-dobrochesnist/

## Approval

| Approved by | Date, signature | Head of the department<br>Bohdan VOROBYOV |
|---|---|---|
| | Date, signature | Guarantor of the educational program<br>Mykola ANISHCHENKO |