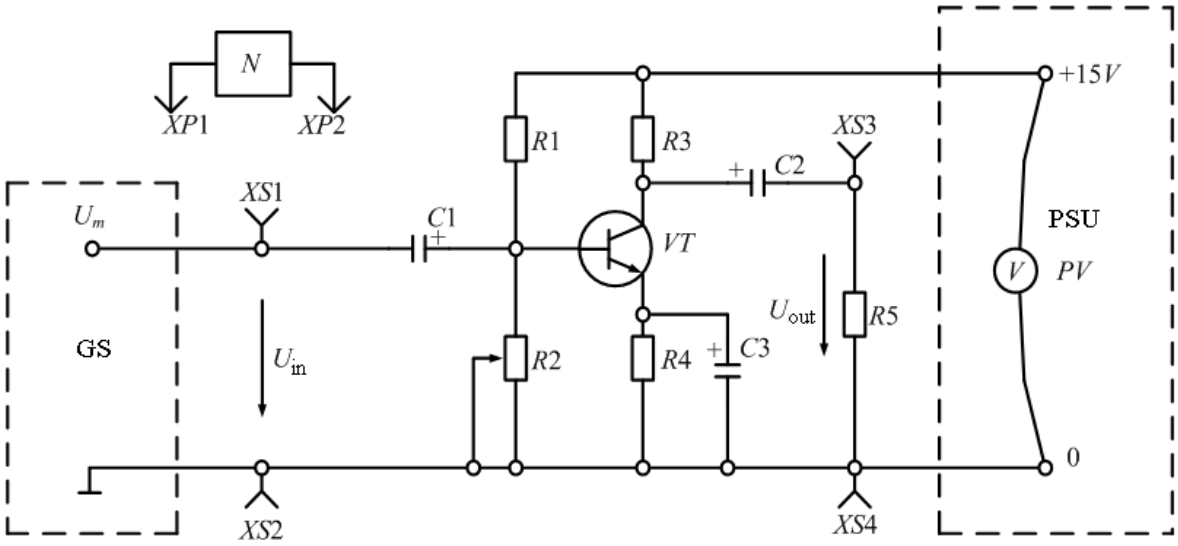
MINISTRY OF EDUCATION AND SCIENCE OF UKRAINE

NATIONAL TECHNICAL UNIVERSITY
«KHARKIV POLYTECHNIC INSTITUTE»

ELECTRONICS AND MICROPROCESSOR TECHNOLOGY

LABORATORY MANUAL ON ELECTRICAL ENGINEERING
Part III



Kharkiv 2024

EDUCATION AND SCIENCE MINISTRY OF UKRAINE

NATIONAL TECHNICAL UNIVERSITY
«KHARKIV POLYTECHNIC INSTITUTE»

DEPARTMENT OF APPLIED ELETRICAL ENGINEERING

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ELECTRONICS AND MICROPROCESSOR TECHNOLOGY

LABORATORY MANUAL ON ELECTRICAL ENGINEERING

In three parts
Part III

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Е 50 **Electronics and microprocessor technology**: **laboratory manual on electrical engineering. In three parts. P. III** / V.F. Boliukh, V.S. Markov, E.V. Honcharov and others. – Kharkiv: NTU "KhPI", 2024. – 96 p.

The course of five laboratory works from the section "Electronics and microprocessor technology" of the discipline "Electrical engineering, electronics and microprocessor technology" has been presented in the form of a complex independent work for preparation for the execution of these laboratory works. Theoretical material on the design and principle of operation of devices, as well as the methodology for their calculation, are provided. The laboratory manual has been intended for independent work of students in the preparation and execution of laboratory, calculation and graphic works, preparation for tests and exams. Part I was published in 2022, Part II was published in 2023.

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УДК 621.3.011.7

INTRODUCTION

The proposed laboratory works are component of the educational process and intended for full-time, part-time and distance learning students.

It involves the consistent acquisition of knowledge related to the study and calculation of electronic devices.

The purpose of laboratory classes is to consolidate theoretical knowledge and acquire practical skills in drawing up electric circuits and turning on different electronic devices, measuring currents and voltages.

On the basis of these studies, calculations of electronic devices are carried out, as well as analysis of research results.

In the laboratory workshop, the safety rules for performing laboratory works, the procedure for their implementation, theoretical provisions, the design and content of the report, and the diagrams for connecting electronic devices and devices are given.

DESCRIPTION OF THE UNIVERSAL LABORATORY BENCH FOR PERFORMING A LABORATORY WORK ON ELECTRONICS

The K4824 universal laboratory bench was intended for carrying out laboratory works from the section "Electronics and microprocessor technology" using the frontal method. The bench is contained in a portable case with a hinged top cover. It is powered by a single-phase AC source of 220 V, 50 Hz. Connecting to the source is done using an electric cord with a standard two-pole plug.

The working field of the bench is shown in Fig. 1. It is divided into the following zones: the power supply unit (PSU – «БЖ» in Fig. 1), the signal generator panel (SGP – «ГС» in Fig. 1), the mounting panel and the panel with electric measuring devices. On the panels of the power supply unit and the generator there are control bodies, indications and sockets for the PSU and SGP outputs. Toggle switch "network-on" («ввімкн. мережа» in Fig. 1), placed on the power supply unit, voltage is applied (the light indicator lights up) to the power supply unit. Across its terminals "~ 8 V"; "~ 24 V" appears alternating voltages of 8 V and 24 V with a frequency of 50 Hz; across terminals "5 V" - direct stabilized unregulated voltage of 5 V; across the terminals "+ 15 V" and "- 15 V" relative to the common output "0" – regulated voltages from 5 V to the specified maximum values of + 15 V and - 15 V (the control knobs "+ 15 V" and "- 15 V" are intended specifically for this).

The voltmeter, located on the PSU panel, can be connected with the handle "+5V; -15V; +15V" to the corresponding sources of constant voltage for its control.

The limit values of the current supplied to the load by any of the sources of the power supply unit should not exceed 0,1 A!!!

The SGP produces voltages of various forms, which are applied to the terminals «U_m» and «⊥». This generator is turned on by the "SGP-on" toggle switch, while the corresponding light indicator lights up. The selection of the voltage form of

the SGP signal is carried out with a handle, next to which the voltage forms generated by it are depicted (rectangular, triangular, sawtooth, sinusoidal).

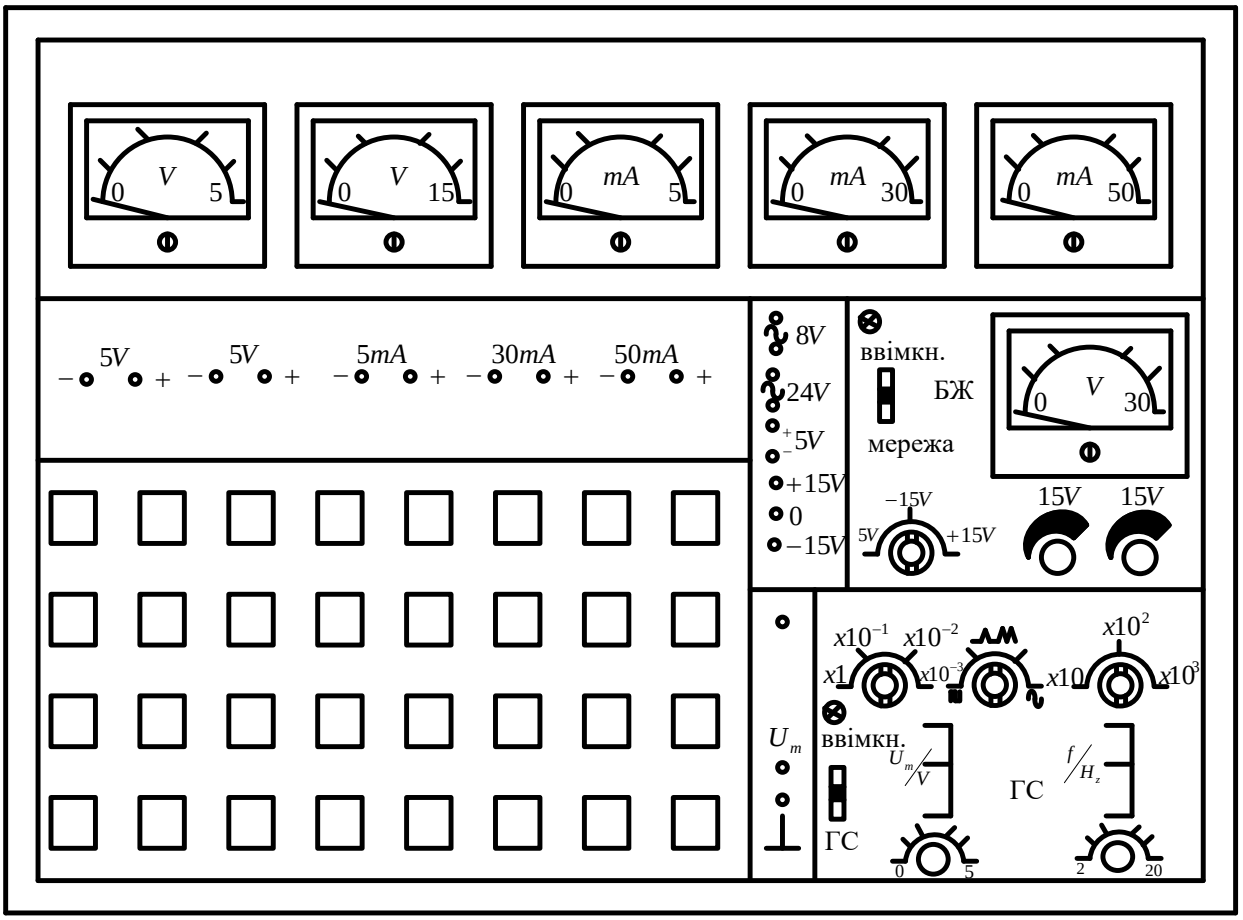


Figure 1 – Universal laboratory bench K4824

The magnitude of the output voltage of the signal is regulated by the knobs marked "U_m / V" (stepwise and smoothly within the range of 0...5 V), and the frequency of the signal - by the knobs marked "f / Hz" (stepwise and smoothly within the range of 20...20000 Hz).

The signal parameters set by the knobs are approximate, their values must be determined by appropriate measuring devices.

Two voltmeters and three milliammeters of the magnetoelectric system are fixed on the panel of electric measuring devices, which can measure constant or rms values of quantities. This panel can be installed at an angle of 0...30° relative to the surface of the bench body (for convenience of measurements).

Observation of the form of variable signals and measurement of their parameters is carried out with the help of electric measuring devices that are not included in the bench (oscilloscopes, electronic voltmeters).

The mounting field, which occupies most of the panel of the bench, contains mounting sockets connected by four to each other. Each such group is an electrical node that allows you to connect up to four elements.

Electric elements and semiconductor devices (resistors, capacitors, diodes, thyristors, transistors, etc.) are contained in transparent plastic boxes with electric terminals, which have inscriptions with information about the type of element and its parameters. They can be connected to each other directly at nodes or using conductors with plug contacts.

SAFETY TECHNIQUES DURING IMPLEMENTATION A LABORATORY WORK

Laboratory benches are active electric circuits and electrotechnical devices, which under certain conditions can become sources of electric shock. In order to create safe working conditions in the laboratory and prevent the possibility of damage to electric equipment, students must know and strictly follow the following rules:

1. Before starting work, make sure that all power sources are in the "OFF" position, and the slider of the autotransformer is set to the zero position.
2. It is strictly forbidden to touch uninsulated wires, connecting clamps and other live parts of electric circuits.
3. Assembling of the electric circuit of the electric device and any connections must be made with the power sources turned off.
4. It is strictly forbidden to turn on the laboratory bench without checking the electric circuit by the tutor.
5. If the network voltage disappears during operation, you should immediately turn off the laboratory bench and set the slider of the autotransformer to the position corresponding to the minimum voltage.
6. Disassemble the circuit only with the permission of the class tutor.
7. If any malfunction is detected in an electric device that is under voltage, it is necessary to turn off the test bench from the network immediately using the emergency shutdown button. This case should be reported to the class tutor immediately.

THE PROCEDURE FOR PERFORMING A LABORATORY WORK

To perform the work, academic groups of students are divided into subgroups of 2 - 4 students. Laboratory work is carried out by the frontal method, that is, all subgroups simultaneously perform the same work, but at different laboratory benches.

To perform laboratory work, each student should prepare a test protocol (draft) in advance, which contains an electric circuit of the experiment and a table of measurements. Before starting the experiments, the subgroup should get acquainted at the workplace with the experimental installation, power sources, electric loads and devices that are used.

During the assembly of the circuit, it is recommended to assemble the main electric current circuit with the inclusion of the receivers to be investigated and the

current circuits of ammeters, wattmeters and phasometers. Then you can connect circuits of voltmeters, wattmeters and phasometers, which are turned on in parallel with the loads. It is necessary to remember the rule that the terminals of devices are used only for their inclusion in the circuit. Nothing else is connected to these terminals, and all additional connections are made to free terminals on the bench panel.

The completed circuit must be shown for verification; power sources should be switched on only with the tutor's permission.

The results of all primary measurements and calculations are recorded in previously prepared tables.

At the end of the experiment, the power sources are turned off, and the measurement results are submitted to the class leader for verification.

If the results of the experiment are recognized by the tutor as correct, the electric circuit is disassembled and the next circuit is drawn up. After the research is completed, the workplace is organized, the conductors and devices are handed over to the place of their storage.

FORMATION AND CONTENTS OF THE REPORT ON A LABORATORY WORK PERFORMED

The report on laboratory work is written by each student separately and must be neat, completed in accordance with the established form.

The report begins with a title page, a sample of which is given on page 7. On the following pages, it is necessary to indicate:

- electric circuits of the experiment;
- rated data of devices under investigation, necessary for writing the report;
- formulae and dependencies used for calculations;
- tables of measurement data and calculation results in accordance with the requirements specified in the methodical instructions for each laboratory work;
- graphic material (graphs, diagrams, drawings);
- analysis results and work conclusions.

Schematic diagrams are drawn using tools according to DSTU (The Ukrainian Standard). Conventional values of typical elements and their sizes are given in the Table 1. It is advisable to build graphs of dependencies obtained on graph paper with standard letter designations of values and measurement units on the axes.

Phasor diagrams must be drawn at the selected scale.

The report is accepted by the lecturer on the day when the next work is performed. At the same time, the student must analyze the obtained results, answer control questions and solve problems according to the topic of the work.

Ministry of Education and Science of Ukraine

National Technical University
«Kharkiv Polytechnic Institute»

Department of Applied Electrical Engineering

Report on laboratory work №

_____

(the title of the work)

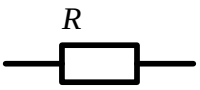
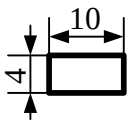
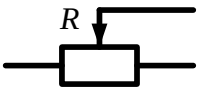
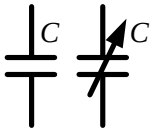
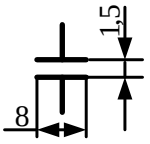
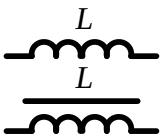
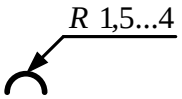
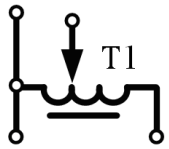
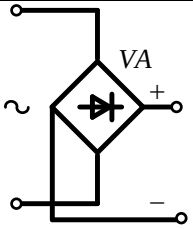
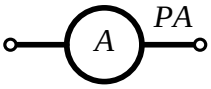
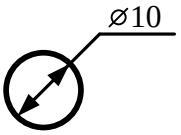
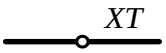
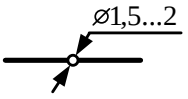
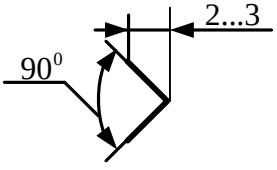
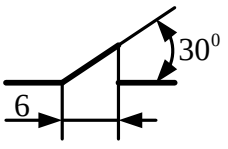
Work was performed by:
student_____; group_____;
(surname, initials) (index) (execution date)

The report was accepted on_____Lecturer_____
(date) (position, surname, initials)

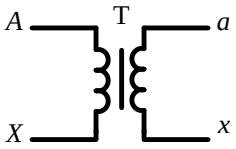
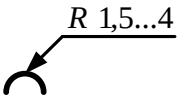
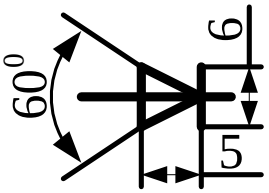
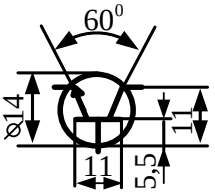
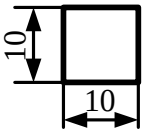
Kharkiv

(Year)

Table 1 – Legend of functional elements in electric circuits

Title of elements		Designation on a schematic diagram я	Dimensions, mm
Resistor	constant resistance		
	variable resistance		
Capacitor of constant and variable capacitance			
Inductive element, inductance Inductor (air-core coil) Inductor (iron-core coil)			
Adjustable autotransformer			
Single-phase semiconductor bridge rectifier			
Electric meters: *PA* – ammeter; *PV* – voltmeter; *PW* – wattmeter; P_{φ} – phase meter			
Joints	separable		
	non-separable		
Contacts of detachable connection (male connector – *XP* and female connector – *XS*)			
Contacts of switching equipment (*Q* – in the power circuits; *S* – control, alarm system)	make		
	break		
Current	direct		
	alternating		

Continuing of Table 1

Title of elements	Designation a schematic diagram	Dimensions, mm
Single-phase double-winding transformer		
Diode		
Zener diode		
Thyristor (dynistor)		
Transistor (*n-p-n* type)		
Measuring oscilloscope		

Laboratory work 11

RESEARCH OF SEMI-CONDUCTOR RECTIFER DIODE, ZENER DIODE AND DYNISTOR

11.1. Purpose of the work

The purpose of the work is to study the design and operation principle of the semi-conductor rectifier diode, Zener diode (stabilitron) and dynistor (uncontrolled thyristor), as well as the experimental study of the current-voltage characteristics (CVC) of these devices.

11.2. Theoretical provisions

The main physical processes in semiconductor devices are the generation of charge carriers, control of their concentration and movement. These processes are formed with the help of electrophysical properties of semiconductor materials that are part of all semiconductor devices.

Germanium Ge, silicon Si, selenium Se, as well as semiconductor compounds such as gallium arsenide, silicon carbide, cadmium sulfide, etc., are most widely used in semiconductor technology.

Charge carriers in semiconductors are electrons and holes. Accordingly, electron and hole conductivity are distinguished. The formation (generation) of a pair of charge carriers (electron-hole) in a semiconductor occurs under the influence of external factors, such as an increase in temperature, the action of an external electric field and light, etc.

The concentration of electron-hole pairs in a semiconductor is determined by the balance between the processes of generation of pairs and their recombination (in-connection of pairs). Such a concentration forms the intrinsic electric conductivity of the semiconductor, which increases as the action of external factors increases.

Under normal conditions, the intrinsic electric conductivity of semiconductors is quite small compared to the electric conductivity of conductors. So, for example, 1 cm^3 of pure germanium at room temperature contains $2{,}5\cdot10^{13}$ pairs of electron-holes with a total number of atoms of $4{,}2\cdot10^{22}$, while 1 cm^3 of the metal contains 10^{22}–10^{23} atoms and the same number of charge carriers (electrons).

Impurities are used to increase the electric conductivity of semiconductors. Materials of the third group of Mendeleev's periodic table of elements (gallium Ga, indium In) or the fifth group (antimony Sb, phosphorus P) are used as impurities. The addition of a small (10^{-5}–10^{-6} %) but precisely set amount of impurities to a pure semiconductor ensures a multiple (10^3–10^5 times) increase in additional carriers compared to the charges related to the conductor's own electric conductivity. At the same time, the impurity gives the semiconductor a sharply pronounced character of electron or hole conductivity. Electron impurity conductivity occurs in a

semiconductor when the impurity has one more valence electron than the semiconductor. In this case, the semiconductor is called an N-type semiconductor, and the impurity is called a donor.

Hole impurity electric conductivity occurs in a semiconductor when the impurity has one valence electron less than the semiconductor. In this case, the semiconductor is called a P-type semiconductor, and the impurity is called an acceptor. Along with the charge carriers formed in the semiconductor, immobile positive ions appear in the N-type semiconductor (Fig. 11.1, *a*) and negative ions in the P-type semiconductor (Fig. 11.1, *b*).

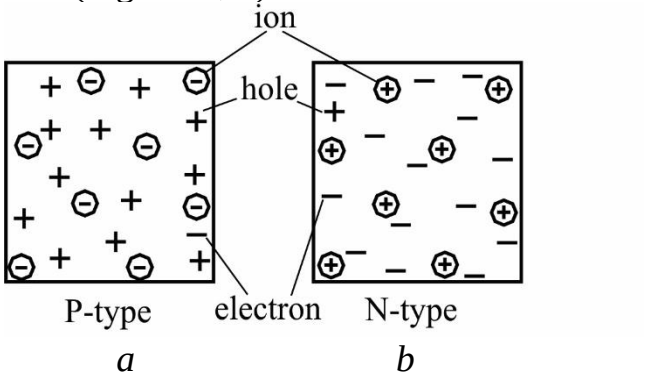


Figure 11.1 – Designation of stationary and mobile charge carriers

Charge carriers in a semiconductor caused by an impurity are called main carriers. In N-type semiconductors, these are electrons, and in P-type semiconductors, they are holes. However, along with the main charge carriers in semiconductors, there are a small number of non-main charge carriers, which are formed by thermogeneration (under the influence of heat) of electron-hole pairs and determine their own electric conductivity.

11.2.1. Properties of *p-n* junction. The principle of operation of most semiconductor devices is based on specific phenomena that occur at the interface between N- and P-type semiconductors, where an electron-hole or *p-n* junction is formed in the adjacent thin layer. The type of semiconductor is determined by its main charge carriers caused by the presence of an impurity. An N-type semiconductor contains electrons, and a P-type semiconductor contains holes. Let's consider these phenomena using Fig. 11.2.

Due to the different concentration of the main charge carriers on both sides of the semiconductor interface, a part of the holes from the boundary region of the P-type semiconductor diffuses (penetrates) into the N-type semiconductor, and a part of the electrons from the boundary region of the N-type semiconductor diffuses into the P-type semiconductor. As a result, a layer of immobile ions is formed along the boundary of the distribution of semiconductors, in which there are no mobile charge carriers, and as a result, such a barrier layer has a high electric resistance. The thickness of the barrier layer *l* usually does not exceed several microns (Fig. 11.2).

The expansion of the barrier layer is hindered by immobile ions of impurities that form an electric double layer. This layer determines the contact potential difference $\Delta\varphi$ (potential barrier) at the boundary of semiconductors, which is, of

course, 0,3 – 0,5 *V*. The potential difference creates an electric field with a blocking EMF E_{bl} in the barrier layer, which prevents the passage of the main charge carriers through the *p-n* junction and does not prevent the passage of non-main charge carriers through it.

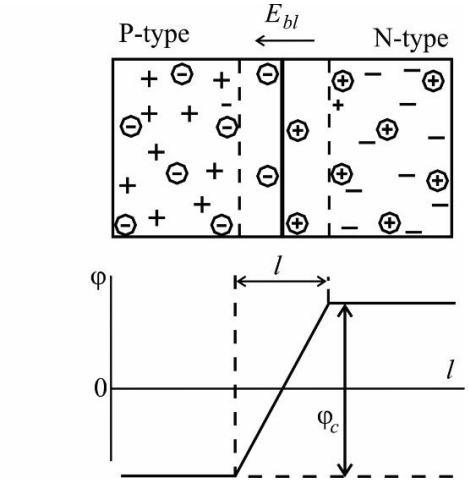
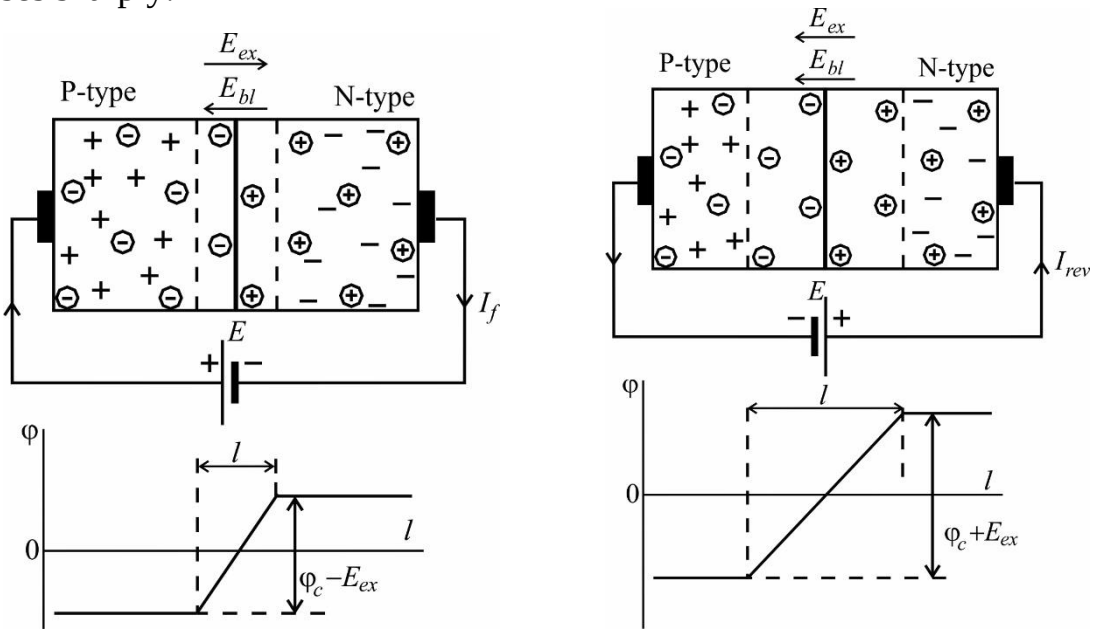


Figure 11.2 – To physical processes in a *p-n* junction

Upon reaching a certain value of E_{bl}, a dynamic equilibrium occurs, in which the strength of the diffusion current I_f, caused by the diffusion of the main charge carriers, becomes equal to the strength of the reverse (drift) current I_{rev}, caused by the movement of non-main charge carriers under the influence of the electric field E_{bl}.

When an EMF source *E* is connected to the *p-n* junction (Fig. 11.3, *a*) in the forward direction ("+" of the source to the P-type region and "–" of the source to the N-type region), the external electric field of the source E_{ex} weakens the field E_{bl}, reduces potential barrier to $\Delta\varphi' = \varphi_c - E_{ex}$ and reduces the thickness of the barrier layer *l*. As a result, the diffusion and with it the current through the *p-n* junction increases sharply.



a *b*

Figure 11.3 – Forward and reverse connection of a *p-n* junction

With the reverse connection of the EMF source to the *p-n* junction (Fig. 11.3, *b*), the external field E_{ex} coincides in direction with the field E_{bl} and thereby contributes to the expansion of the barrier layer to *l* and the increase of the potential barrier to $\Delta\varphi'' = \varphi_c + E_{ex}$. At the same time, the resistance of the *p-n* junction increases sharply, and the current practically does not pass through this junction. Therefore, the *p-n* junction has one-way conductivity, which is practically used in a whole range of semiconductor devices - diodes, transistors, thyristors, etc.

11.2.2. Semiconductor diode. A semiconductor diode is a semiconductor device with one *p-n* junction and two terminals, which uses the property of the *p-n* junction to conduct current well in one direction and poorly in the opposite direction. Diodes designed to convert an alternating current into a direct current are called rectifiers. The structure, conventional designations of the diode and Zener diode are shown in Fig. 11.4, *a*, *b*, *c*.

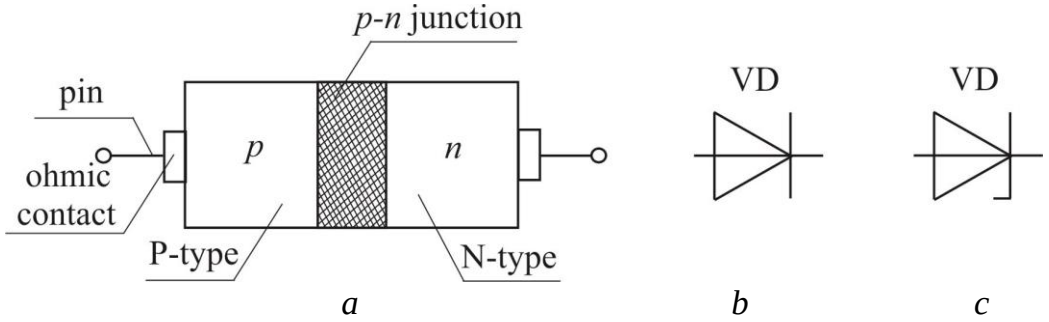


Figure 11.4 – Structure and designations of a rectifier diode and a Zener diode

The properties of a semiconductor diode are determined by the non-linear current-voltage characteristic (CVC) of the open and closed junction (Fig. 11.5).

When the diode is switched on in forward direction, the positive pole of the direct voltage source is connected to the terminal of the P-type semiconductor, and the negative pole is connected to the terminal of the N-type semiconductor. The reverse is the case when it is switched back on. On the sections 1 and 2 of CVC correspond to forward switching of the diode, and sections 3 and 4 to reverse switching. With forward switching, the electric field of the *p-n* junction and the source of constant voltage are directed toward each other, and with reverse switching, they coincide.

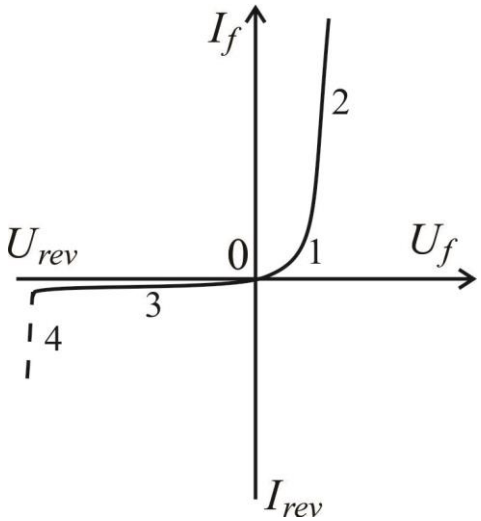


Figure 11.5 – The current-voltage characteristic of a rectifier diode

In section 1, the electric field of the *p-n* junction is greater than the electric field of the source and, accordingly, the direct current is insignificant. In section 2, the external field of the source is greater than the blocking field of the *p-n* junction, there is no blocking layer, the current is determined only by

the resistance of the semiconductor. This resistance is relatively small, which leads to a slight voltage drop at the *p-n* junction ($U_f \leq 1{,}2$ V). The forward current is a diffusion current.

In section 3, the blocking layer of the *p-n* junction prevents the movement of the main carriers. The resistance of the closed *p-n* junction is relatively large, and the external voltage of the source falls entirely on it. A small current determines the movement of non-basic charge carriers (electrons of a P-type semiconductor and N-type holes). This reverse current is called a drift current. It is due to the fact that for a number of non-basic carriers, the blocking field creates a force and acceleration sufficient to overcome the *p-n* junction. In section 4, a *breakdown* of the *p-n* junction occurs and the reverse current increases rapidly. This is due to the fact that when moving through a *p-n* junction under the influence of an electric field, non-main charge carriers acquire energy sufficient for impact ionization of semiconductor atoms. In the transition, the avalanche multiplication of charge carriers begins. This type of *electric breakdown* is called an *avalanche*. It develops in lightly doped semiconductors with a relatively wide *p-n* junction. In heavily doped semiconductors, the width of the *p-n* junction is relatively small, which prevents the occurrence of an avalanche breakdown due to insufficient energy for impact ionization, acquired by moving carriers. In this case, an electric breakdown of the *p-n* junction may occur.

If the temperature of the *p-n* junction increases as a result of its heating by current and insufficient heat dissipation, then the generation of pairs of charge carriers increases, which leads to a further increase in the reverse current, heating of the *p-n* junction and can cause its destruction. Such a process destroys the *p-n* junction and is called a thermal breakdown.

The limitation of the value of the forward current I_f is due to the thermal destruction of the diode, and the value of the reverse voltage U_{rev} is due to thermal breakdown and the destruction of the rectifying properties of the diode. Both of these quantities are the main parameters of diodes.

According to the design of the *p-n* junction, semiconductor diodes are divided into point and planar. A point diode is a device with a very small area of electric transition, which can be obtained by fusing a metal needle with an impurity applied to it into a semiconductor plate with a certain type of electric conductivity. At the same time, impurities diffuse from the needle into the main semiconductor, which create an area with a different type of electric conductivity. Thus, a miniature *p-n* junction is created near the needle. Due to the small area of the *p-n* junction, the point diode belongs to low-power devices. The permissible dissipation power of this type of diode is of the order of 10 mW at a value of the forward current of the diode of 10 – 20 mA.

11.2.3. Semiconductor Zener diode. Semiconductor Zener diode (planar diode, stabilitron) is a semiconductor diode, the voltage on which in the area of *electric breakd*own depends weakly on the current strength and which is used to stabilize the voltage.

Zener diodes are manufactured as silicon planar diodes. Planar diodes and Zener diodes are devices with a significant area of the *p-n* junction obtained by fusing semiconductor plates with different types of charge carriers or diffusion of impurity atoms into the original semiconductor plate. In Fig. 11.6 shows the design of a Zener diode. The semiconductor crystal plate 1 is soldered to the crystal holder 2, so that a contact is formed. Outputs 4 and 5 are made from this contact and electrode 3, and the upper output 4 passes through the glass pass-through insulator 6 into the housing 7 and the tube 8.

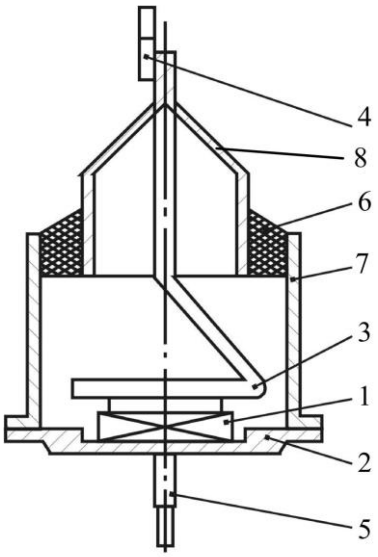


Figure 11.6 – Design of a Zener diode

Flat diodes of low dissipation power ($P = 1$ W, $I_f \leq 1$ A) are used in automation and instrument engineering. High-power diodes ($P = 10$ kW, $I_f \leq 2$ kA) are used mainly in rectifiers.

The phenomenon of *electric breakdown*, which is dangerous for ordinary diodes, finds a useful application in silicon planar diodes, which have received the name of silicon zener diodes or reference diodes. The CVC of the Zener diode is shown in Fig. 11.7.

The normal mode of operation of Zener diodes is operation when the *p-n* junction is reversed. The stabilization section is located on the CVC of the stabilizer from $I_{st.\min}$ to $I_{st.\max}$. The value of the minimum stabilization current is limited by the non-linear section of the reverse part of the CVC of the Zener diode. The value of the maximum stabilization current is the permissible temperature of the semiconductor. In the area of stabilization, the voltage drop across the Zener diode practically does not change, which allows you to use the device as a voltage stabilizer.

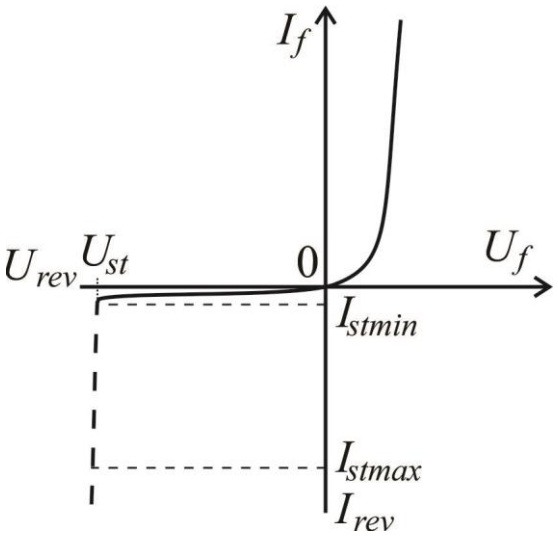


Figure 11.7 – The current-voltage characteristic of a Zener diode

The direct current circuit of the zener diode is similar to the corresponding current circuit of the diode.

The main parameters of the Zener diode:

1) stabilization voltage U_{st} – the voltage drop across the Zener diode in the stabilization area at a normal value of the current;

2) the minimum stabilization current $I_{st.\min}$ is the value of the current through the stabilizer diode, at which a stable *avalanche breakdown* occurs;

3) maximum stabilization current $I_{st.\max}$ – the largest value of the current through the zener diode, at which the dissipation power across the Zener diode does not exceed the permissible value;

4) differential resistance R_{dif} in the area of stabilization, which characterizes the degree of voltage stability when the current changes in the area of the avalanche breakdown;

5) the maximum dissipation power P_{max} is the largest power released in the *p-n* junction, at which the thermal breakdown of the *p-n* junction does not occur.

11.2.4. Semiconductor thyristor (dynistor). A thyristor is a conductor device with two stable states, which has three (or more) *p-n* junctions and can be switched from a closed state at the same time.

Thyristors with two terminals are called single or dynistors (uncontrolled thyristors), and with three-terminal or treenistors (controlled thyristors).

Fig. 11.8 *a*, *b* shows the structure of a threenistor and a dynistor, and also the designation of a dynistor. The control electrode in a threenistor is called a gate. The structure consists of four sections of the conductor with electric conductivity types p_1-n_1-p_2-n_2, which are combined and between, which three electron cores are created, the $P1$, $P2$, $P3$ junctions are situated.

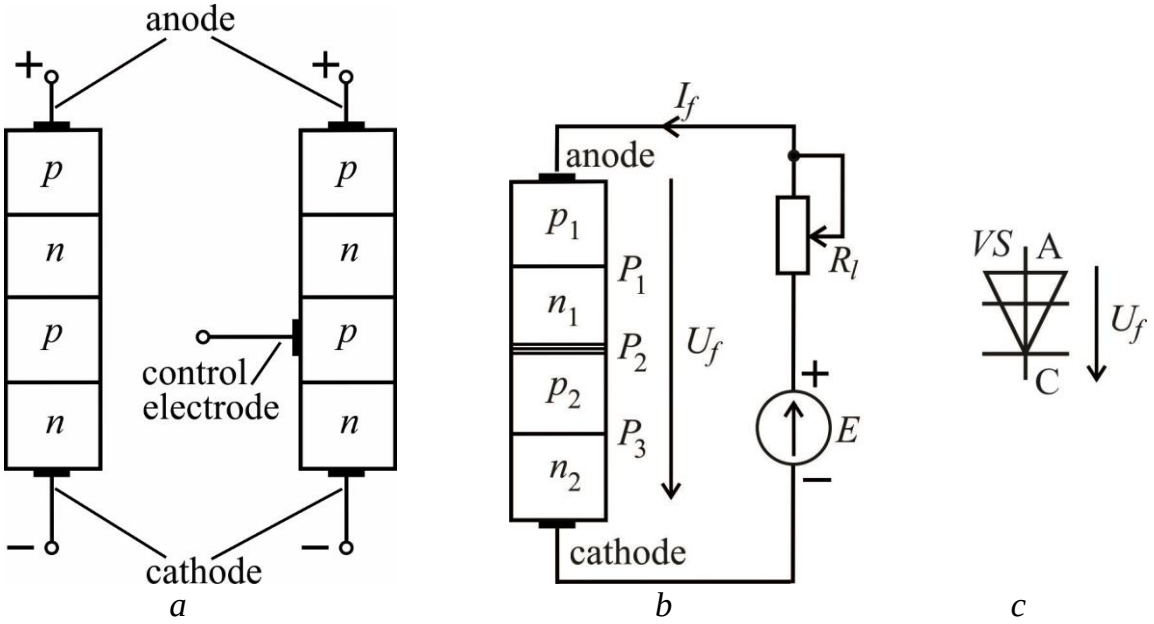


Figure 11.8 – A stuctural diagram of a threenistor (*a*), a dynistor (*b*) and designation of a dynistor

The outer layers of the thyristor p_1 and n_2 are made with low resistance (with a large number of impurities), as a result of which they are enriched with the main carriers of charges, and the internal layers p_2 and n_1 are made with high resistance (with a small number impurities), that they are imbued with similar charge carriers. When switched on in the forward direction, the voltage is supplied to the thyristor in such a way that junctions $P1$ and $P3$ are switched on in the forward direction, and junction $P2$ is switched on in the reverse direction. Therefore, the maximum voltage U drops across the closed junction $P2$. Apparently, the thyristor closes and passes a small flow at the $P2$ junction, which creates a non-main charge carrier.

With an increased voltage U that is applied to the thyristor (which is within the reach of larger EMF of the source), the flow of the thyristor increases

significantly, so that the thyristor behaves as a voltage under the return voltage. This is shown on the current-voltage characteristic by section 1 (Fig. 11.9).

While the thyristor is closed, the electric field of the external voltage appears on the charge in the *P2* junction, but the stronger electric field at the thin sphere of the *p-n* junction increases the fluidity of the flow of electrons and have a nice run. When the voltage reaches a critical value of the forward voltage or the breakdown voltage U_{bo} which brings the thyristor CVC to the point **A** (Fig. 11.9), the fluidity of the charge becomes sufficient for the alignment of the valence bonds of the atoms on the conductor. There is an avalanche-like increase in the number of charge carriers and ionization of the *P*2 junction; the internal layers of the thyristor carry a charge from the external low-impedance layers. The current grows sharply and is surrounded only by the load resistor R_l. The voltage across the R_l increases, and across the thyristor decreases. Therefore, the differential operation R_{dif} will be negative. This mode of the thyristor is unstable and demonstrates part between points **A** and **B** on the CVC (dash line in Fig.11.9). The thyristor spontaneously switches on to "On-state" position (point **B**). After a breakdown, the voltage on the thyristor drops to 0,5 – 1 V, therefore, an avalanche breakdown at low voltage and high flow does not cause irreversible processes in the thyristor structure.

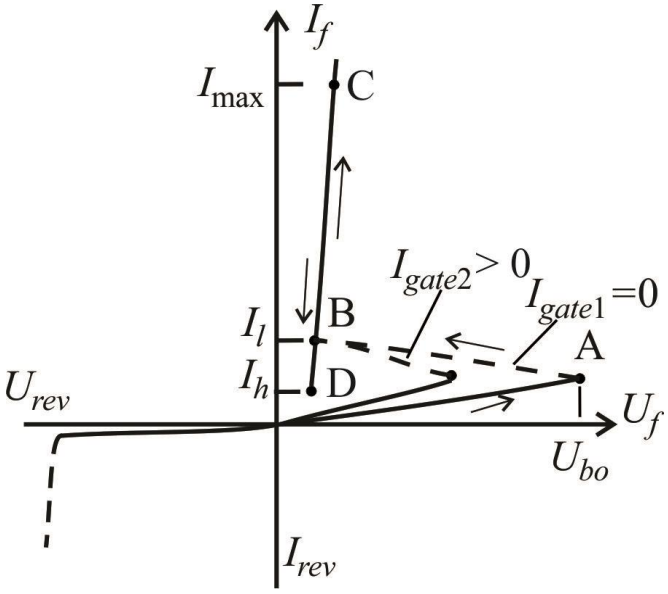


Figure 11.9 – The current-voltage characteristic of a dynistor

The point **B** is characterized by the latching current. It is minimum forward current required to maintain a thyristor in the "On-state" immediately after switching from the "Off-state" to the "On-state" has occurred and the triggering signal has been removed.

With a further increase in the voltage of the power source *E* or the changed load R_l current of the thyristor continues to increase, the voltage across the new one changes slightly, which indicates part **BC** of the thyristor CVC. At this part, the static resistance of the thyristor $R_{st} = U/I$ is small.

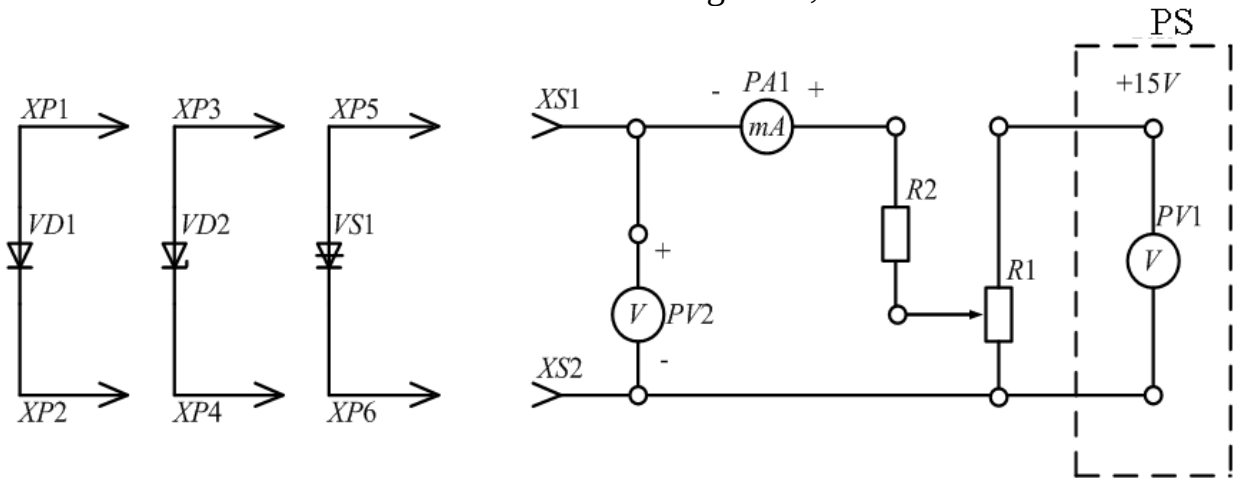
The point **C** is the maximum current in "On-state". The point **D** is the holding current minimum current required to maintain a thyristor in the "On-state" position. If we have threenistor or controlled thyristor, then the bigger value of the current of the gate I_{gate} (control electrode), the lower value of the breakdown voltage we have and the faster the thyristor appears in "On-state".

When the thyristor is reversely connected, the dynistor is in a closed state, so junctions *P*1 and *P*3 are located in the non-conductive direction. There is a reverse voltage between them and therefore no breakdown is detected. The static resistance

of the thyristor at this stage of the CVC is large. To overcome the breakdown of the thyristor, which fails the thyristor due to possible thermal breakdown, it is necessary that the reverse voltage value should be less than the maximum allowed value.

11.3. Object of study

The schematic diagram of the experiment electric circuit is shown in Fig. 11.10. Rectifier diode VD1, Zener diode VD2 and VS1 dynistor, which are dual-electrode semiconductor devices, are shown, respectively, in Fig. 11.1, *a, b, c*; power circuit and measurement devices are shown in Fig. 11.1, *d*.



a *b* *c* *d*

Figure 11.10 – The shematic diagram of the experiment electric circuit

The power supply (PS) is equipped with a voltmeter voltage regulator 15 or 30 volts. The power supply voltage is measured by a *PV*1 voltmeter. Adjusting the voltage can be done by the additional resistor R_1 (2,2 kOhm), which is switched on as the potentiometer circuit is used to limit the current, the ballast resistor R_2 (300 Ohm). The *PA*1 mini ammeter and *PV*1 voltmeter are used for measurement current and voltage across diodes. The devices will be connected to XS1 and XS2 sockets by XS1 and XS2 pins in forward direction.

Each device should be switched on two times: first – as shown in Fig. 11.1, the other in reverse direction for this it's enough to turn on a device by 180 degrees, i.e. swap its pins.

The main parameters of the considered devices are given in Table 11.1, 11.2 and 11.3.

Table 11.1

Type of the rectifer diode	Forward current, A	Forward DC voltage, V	Reverse maximum voltage $U_{rev.max}$, V	Direct reverse current at $I_{rev.max}$, mA
КД209А	0,1	1,0	400	0,1

Table 11.2

Type of the Zener diode	Stabilization voltage U_{st}, V	Minimal current of stabilization, mA	Maximal current of stabilization, mA	Direct maximum current, mA	Differential resistance, Ohm
Д814А	7...8,5	3	40	50	6

Table 11.3

Name of the dynistor parameters type КН102Г	Parameters value
Limited forward current in the on-state condition $I_{f\max}$, mA	200
Forward voltage in the on-state condition at $I_{f\max}$, U_f, V	1,5
Minimum current in the on-state condition $I_{f\min}$, mA	15
Constant maximum direct voltage in the off-state condition $U_{c.s.max}$, V	14
Constant current in the off-state condition at $U_{c.s.max}$, $I_{c.s.}$, μA	80
Maximum constant reverse voltage $U_{rev.max}$, V	10
Reverse current at $U_{rev.max}$, I_{rev}, mA	0,5

11.4. The order of the experiment execution

Before the assemble of the circuit, it is necessary to connect the laboratory bench to the network, turn on the “network-on” toggle switch, and set the minimum value of the power supply to the voltmeter *PV*1 of the bench. Turn off the toggle switch. Assemble of the circuit in accordance with Fig. 11.10, d and set the minimum value of voltage at the output of potentiometer *R*1 by voltmeter PV2.

11.4.1. Research of a rectifer diode. Connect the rectifier diode VD1 in the forward direction (Fig. 11.10, *a*, *d*).

By changing the current from zero to the maximum value using the potentiometer *R*1 and the regulator of the power supply unit, read the forward branch of the CVC of the diode I_f (U_f) (7-8 points). The values of current I_f and voltage U_f must be written down in Table 11.4.

A sample of the CVC of the rectifier diode is shown in Fig. 11.5.

Table 11.4

U_f, V	0							
I_f, mA	0							
U_{rev}, V	0							
I_{rev}, mA	0							

Turn off the voltage and reverse the diode. To carry out the read of the reverse branch of the CVC named I_{rev} (U_{rev}), changing the voltage from zero to the maximum possible value (it is enough 3-4 points). Write down the results of the measurements in Table 11.4.

11.4.2. Research of a Zener diode. Instead of the rectifier diode, connect the VD2 Zener diode to the circuit (Fig. 11.10, *b*, *d*).

In this experiment it is necessary to take into account that on the reverse branch of the CVC suddenly arises and the current stabilizes rapidly, while the voltage changes very slowly (the working part of the CVC of the Zener diode). A sample of the CVC of a Zener diode is shown in Fig. 11.7.

Make characterization of the Zener diode CVC in the same way as for the rectifier diode, but with reverse switching it is already necessary to read 6-7 points. Write down the results in the Table 11.5.

Table 11.5

U_f, V	0								
I_f, mA	0								
U_{rev}, V	0								
I_{rev}, mA	0								

11.4.3. Research of a dynistor. Experimental study of the dynistor is carried out according to the circuit, which is based on Fig. 11.1, *c*, *d*, in this order.

To read the forward branch of the dynistor CVC $I_{\text{f}}(U_f)$. To make this, by increasing the voltage from zero with the help of the potentiometer *R*1, it is necessary to determine the voltage in open condition U_{oc} and the current I_f across the dynistor and enter the results in Table 11.6.

Table 11.6

U_f, V			U_{bo}, V	U_{latch}, V			$U_{f\,\max}$, V	U_{hold}, V	U_{rev}, V		
0									0		
I_f, mA			I_{bo}, mA	I_{latch}, mA			$I_{f\,\max}$, mA	I_{hold}, mA	I_{rev}, mA		
0									0		

Then, by returning to the zero voltage value and changing it from zero to U_f, read the three points of the characteristic and enter this data in the same table. To fix the values of the voltage U_f and current I_{f} in the "On-state" of the dynistor and then read three more points, raising the current to the maximum possible value for this open max. By reducing the current from the maximum value, determine the holding current I_{hold} and the corresponding holding voltage U_{hold}. Make these measurements in Table 11.6.

Measure the reverse of the CVC branch from I_{rev} (U_{rev}), changing the voltage from zero to the maximum possible value (three points is enough). The results of the measurements are also given in Table 11.6. A sample of the CVC of a dynistor is shown in Fig. 11.9.

11.5. Processing the results of the experiment

According to the data contained in the Table 11.4, 11.5, and 11.6, to draw the CVC of a direct diode, a Zzener diode, and a dynistor.

Using these characteristics to calculate the static resistances of a rectifier diode, a Zener diode, and a dynistor at the corresponding sections of the CVC:

1) forward resistance at the highest current value

$$R_f = U_{f\max}/I_{f\max};$$

2) reverse resistanceat the highest voltage value

.

Explain the reason for the difference between the values of the forward and reverse resistances of the devices.

Using the CVC of a Zener diode, calculate the differential resistance on the stabilization part of its CVC

$$R_{\text{dif}} = \Delta U_{\text{st}} / \Delta I_{\text{st}} .$$

Calculate the differential resistance of the dynistor in “Off-state” on a branch of the CVC to the **A** point and on the part with unstable operation from the **A** point to the **B** point (Fig. 11.9).

Control Questions

1. Explain the structure of the *p*-*n* junction of the diode.

2. What is the direct and reverse switching on *p*-*n* junction?

3. What physical processes occur in the *p*-*n* junction with its direct and reverse switching?

4. What types of breakdowns can occur in the *p*-*n* junction, under what conditions and what are their consequences?

5. Explain the phenomenon of capacitance of *p*-*n* junction.

6. Explain the design, operation principle and purpose of the rectifier diode, stabilitron and dynistor.

7. To visualize the CVC of the rectifier diode, Zener diode and dynistor and explain their features.

8. What is the static and differential resistance of diodes and dynistors?

Laboratory work 12

RESEARCH OF SINGLE-PHASE RECTIFIERS

12.1. Purpose of the work

The purpose of the work is to study the principle of operation and experimental study of one- and two-period rectifiers of single-phase sinusoidal current and smoothing filters.

12.2. Theoretical provisions

RECTIFIER is a device that converts alternating current into direct current. The rectifier block diagram is shown in Fig. 12.1.

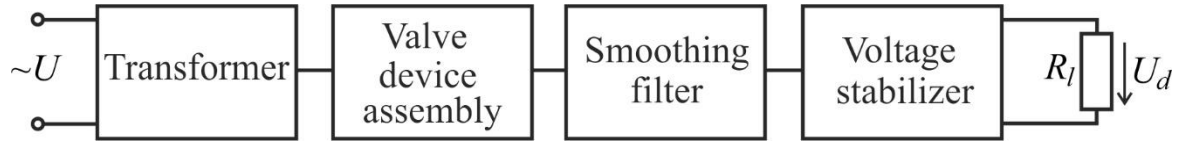


Figure 12.1 – The rectifier block diagram

The transformer regulates the voltage to the required value. *The valve device assembly* (*valve group*) contains elements with one-sided conductivity: rectifier diodes in uncontrolled rectifiers and thyristors in controlled rectifiers. *Smoothing filters* are designed to reduce the ripple of the rectified voltage. *The voltage stabilizer* (*voltage regulator*) keeps the constant voltage across the load resistor R_l.

There are single-phase and three-phase, controlled and uncontrolled rectifiers.

12.3. Single-phase rectifiers

Schematic diagrams, principle of operation, parameters and characteristics

To rectify a single-phase alternating voltage, three circuits are used:

1) a half-wave circuit;

2) a bridge circuit (Grets circuit);

3) a double half-wave circuit or full-wave circuit (with the lead of the midpoint of transformer or using a central tap transformer).

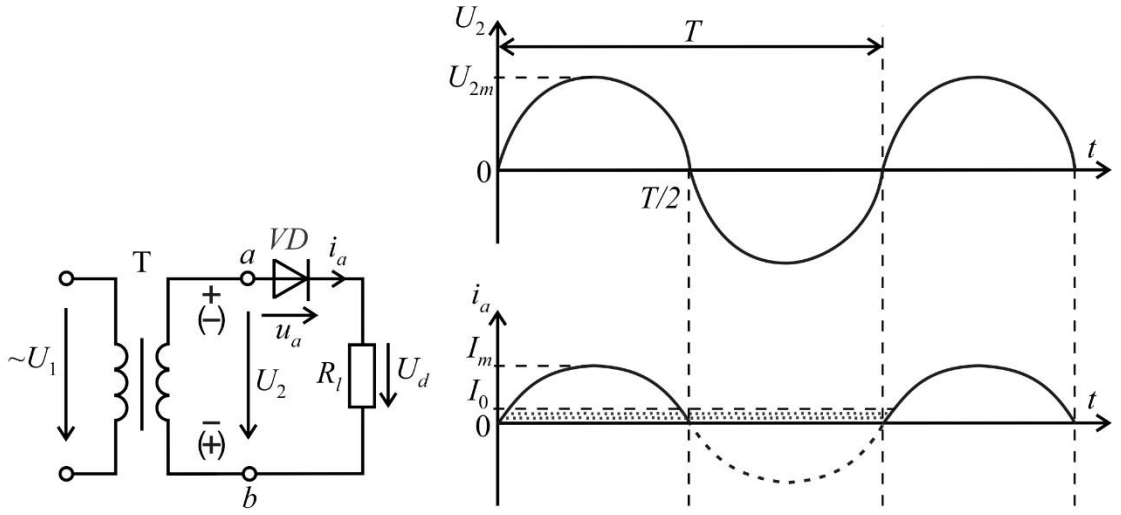
Half-wave circuit in which the current passes through the valve only for one half-period of the alternating voltage of the source. Double half-wave circuits in which the current passes through the valve group for two half-periods of the alternating voltage of the source.

Consider the ratio of the parameters in the rectifiers under the following assumptions:

1) the leakage inductance of the transformer and the resistance of its windings are equal to zero;

2) the resistance of the valve in the forward direction is equal to zero, and in the opposite direction it is equal to infinity.

12.3.1. A single-phase half-wave rectifier. Time diagrams of voltages and currents. The electric circuit of the rectifier and its time diagrams are shown in Fig. 12.2, *a*, *b*.



a *b*

Figure 12.2 – The schematic diagram of a single-phase half-wave rectifier (*a*) and its time diagrams (*b*)

Define the constant component of the rectified current

$$I_0 T = \int_0^{T/2} i_2 dt$$

Since, $i_2 = I_m \sin \omega t$ then

$$I_0 T = \int_0^{T/2} I_m \sin \omega t dt = -I_m \frac{\cos \omega t}{\omega}\Big|_0^{T/2} = 2\frac{I_m}{\omega}$$

$$I_0 = 2\frac{I_m}{\omega T}.$$

But since $\omega = \frac{2\pi}{T}$, i.e. $\omega T = 2\pi$, then

$$I_0 = 2\frac{I_m}{\omega T} = \frac{2I_m}{2\pi} = \frac{I_m}{\pi} \quad \text{or} \quad \boxed{I_0 = \frac{I_m}{\pi} \approx 0{,}318 I_m}.$$

The constant component of the voltage, expressed in terms of the maximum value

$$U_0 = I_0 R_l = \frac{I_m}{\pi} R_l = \frac{U_m}{\pi} = 0{,}318 U_m \ .$$

The constant component of the voltage, expressed in terms of the actual value (root-mean-square or RMS value)

$$U_0 = \frac{U_m}{\pi} = \frac{\sqrt{2}U}{\pi} \approx 0{,}45U$$

Thus, in this circuit, the maximum voltage across the diode

$$U_m = U_{rev} = \pi U_0 = 3{,}14U_0,$$

the voltage across the diode is three times higher than on the load.
The average value of the diode current in this circuit $I_{av} = I_0$.

The ripple value of the rectified voltage is characterized by the ripple factor

$$\boxed{K_r = \frac{U_{1m}}{U_0}},$$

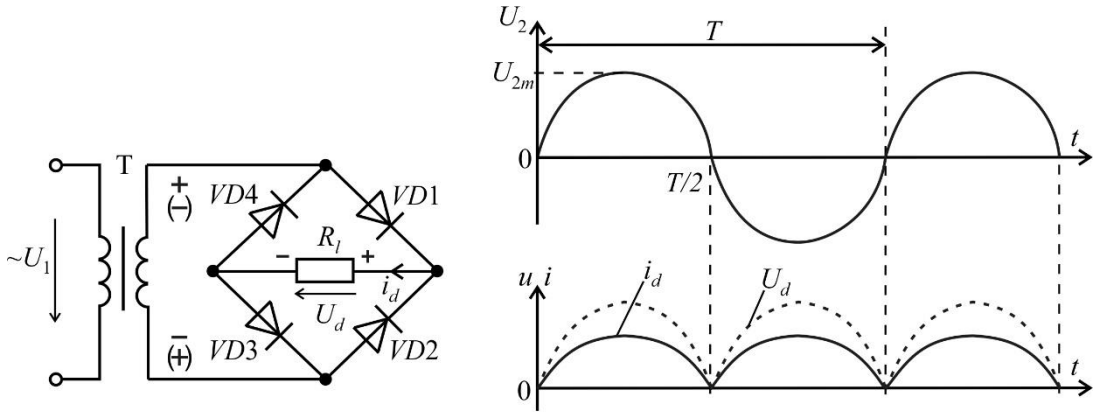
where U_{1m} is the amplitude (peak value) of the variable component of the voltage, changing with the pulse repetition rate, i.e. amplitude of the first harmonic.

For a half-wave circuit

$$U_{1m} = \frac{U_{2m}}{2} = \frac{\pi U_0}{2} = 1{,}57 \cdot U_0, \quad \text{and} \quad K_r = 1{,}57.$$

The disadvantages of the circuit:
1) a large value of the ripple coefficient;
2) the voltage across the load is almost 3 times less than on the diode;
3) the constant component of the rectified current is much less than the current in the secondary winding of the transformer, which leads to its insufficient current use.

12.3.2. A bridge circuit (Grets circuit). The circuit of the rectifier and the time diagrams are shown in Fig. 12.3 *a, b*.



a *b*

Figure 12.3 – The schematic diagram of a single-phase dridge rectifier (*a*) and its time diagrams (*b*)

I_0 is 2 times greater than in a half-wave circuit. Therefore, it is:

$$\boxed{I_0 = 2\frac{I_m}{\pi} \approx 0{,}636 I_m}$$

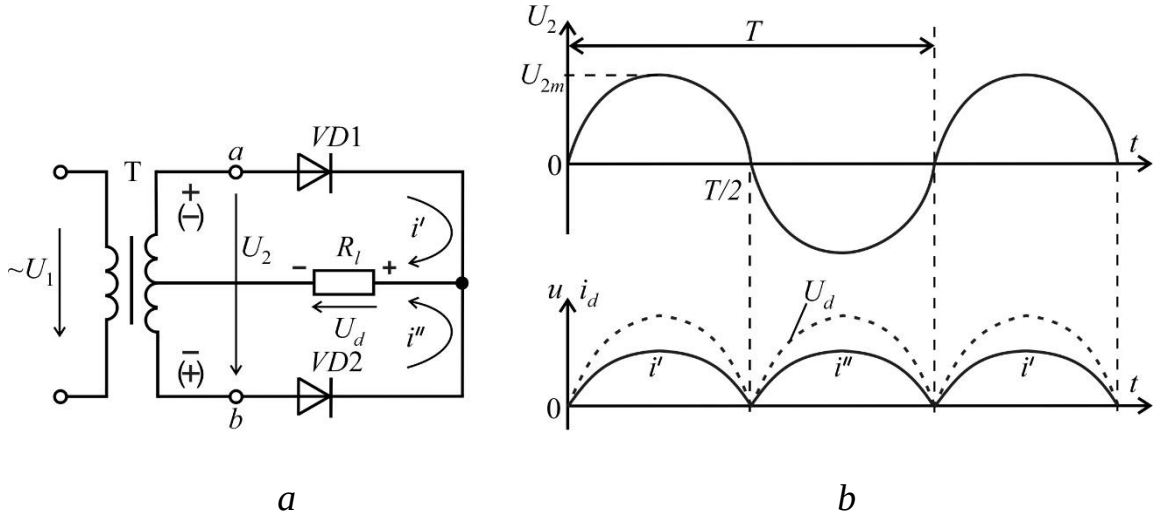
$$U_0 = I_0 R_l = 2\frac{I_m}{\pi} R_l = \frac{2 \cdot U_m}{\pi} = 0{,}636\, U_m$$

$$U_0 = 2\frac{U_m}{\pi} = \frac{\sqrt{2} \cdot 2 \cdot U}{\pi} \approx 0{,}9\, U;$$

$$K_r = 0{,}67\,.$$

The frequency of the rectified current is 2 times higher than that of the network.

12.3.3. A double half-wave circuit with a midpoint output of a transformer. The circuit of the rectifier and time diagrams are shown in Fig. 12.4, *a*, *b*.



a *b*

Figure 12.4 – The schematic diagram of a double half-wave rectifier (*a*) and its time diagrams (*b*)

This is actually a combination of two half-wave rectifiers connected to the load resistor R_l in different phases.

The ratio of the parameters in this circuit are the same as in the bridge circuit.

Advantages of the double half-wave rectifiers over the half-wave rectifiers:

The average value of the rectified current and voltage is 2 times greater, and the ripple is less. But double half-wave rectifiers have a more complex design and cost.

Comparison of the double half-wave circuits:

1) the bridge circuit is structurally simpler, its dimensions, weight and cost are lower than the transformer circuit;

2) the maximum reverse voltage on the closed diodes in the bridge circuit is 2 times less (each of the two diodes accounts for half the voltage);

3) but in the bridge circuit, 2 times more diodes are needed.

When rectifying the currents $I > I_{fr\max}$ for one diode, in parallel, diodes of the same type with additional resistances are included.

The values of the currents are determined by the resistance in the forward direction. But the resistance of the diodes in the forward directions R_f even for the same type of diodes are different. To equalize the currents of the diodes, additional resistances are sequentially included. Moreover, R_d is 5...10 times more than R_f (Fig. 12.5).

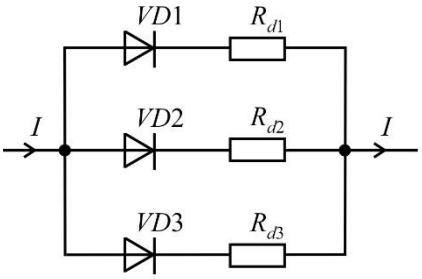


Figure 12.5

When rectifying a voltage exceeding the maximum allowable for the diode $U_{\text{rev·max}}$, a serial connection of diodes shunted by resistors are used. In this case, the reverse voltage across the diodes is distributed in accordance with their inverse resistances R_d. To align the reverse voltages parallel to the diodes, we can include shunt resistors R_{sh}, the value of which is equal to R_{sh} = (0,1...0,2) R_d (Fig. 12.6).

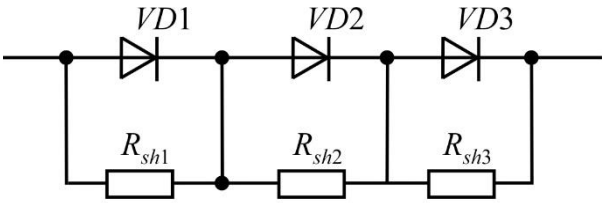


Figure 12.6

Table 12.1 – Parameters of uncontrollable rectifiers with a resistive load

Type of a rectifier	U_0	K_r	$U_{\text{rev max}}$
– half-wave circuit	$0{,}45U_2$	1,57	3,14
– double half-wave circuit with a midpoint output of a transformer	$0{,}9U_2$	0,67	3,14
– bridge circuit	$0{,}9U_2$	0,67	1,57

12.4. Smoothing filters. Schematic diagrams, principle of operation, parameters and characteristics

To reduce the ripple of the rectified voltage, smoothing filters are used. Ripple reduction is estimated by a smoothing coefficient

$$\boxed{q = \frac{K_r}{K_r'}},$$

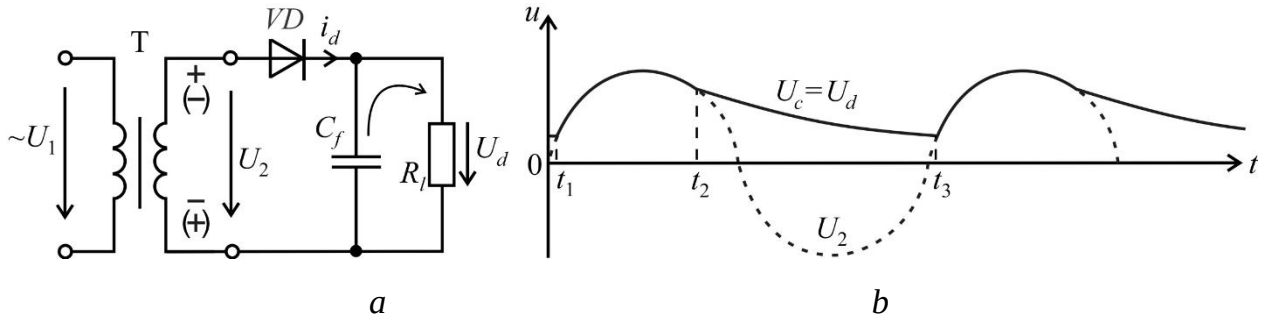
where K_r and K_r' are the ripple coefficients before and after the filter.

The main requirements for smoothing filters are the maximum reduction of the high-frequency components of the currents in the load resistance.

The inductive element $L \Rightarrow X_{Lk} = \omega k L$, and the capacitive element $C \Rightarrow X_{Ck} = \dfrac{1}{\omega k C}$, where *k* is the harmonic number.

Therefore, the inductor is set in series, and the capacitor is parallel to the load.

12.4.1. A capacitive filter. The schematic diagram of the filter is shown in Fig. 12.7, *a*.



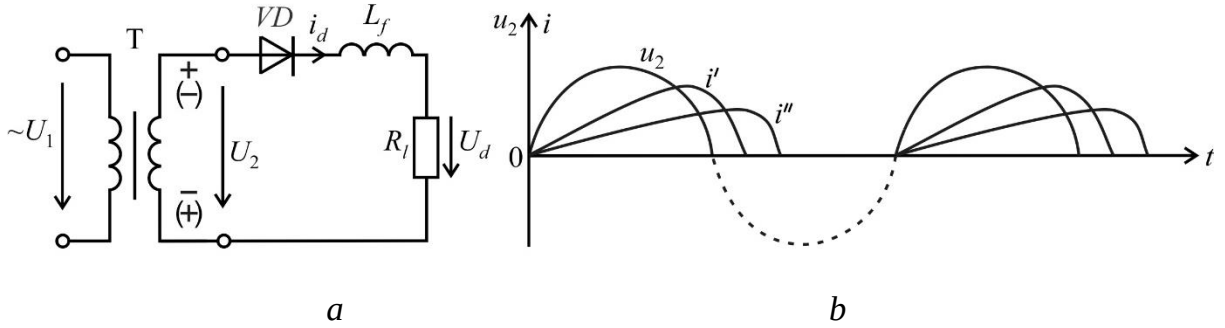
a *b*

Figure 12.7 – The schematic diagram of the capacitive filter (*a*) and time diagram (*b*)

The capacitor is charged to voltage U_2 when $U_2 > U_c$ (interval $t_1 - t_2$) as it shown in Fig. 12.7, *b*. During the time interval ($t_2 - t_3$), the voltage $U_c > U_2$ – the diode is closed, and the capacitor is discharged through the resistor R_l with a time constant.

From the moment of time t_3 $U_c < U_2$ – the capacitor is charging, etc. That is, when the diode passes the current, the capacitor is charged, and when the reverse voltage is applied to the diode, the capacitor is discharged to the load R_l.

12.4.2. An inductive filter. The schematic diagram of the filter is shown in Fig. 12.8, *a*.



a *b*

Figure 12.8 – The schematic diagram of the inductive filter (*a*) and time diagram (*b*)

During the positive half-wave of the voltage u_2, when the current *i* rises, the inductor L_f stores energy, and in the negative half-wave, energy is spent on maintaining the current.

The duration of the current i_l pulses in is determined by the time constant $\tau = \frac{L_f}{R_l}$. The larger the inductance of the smoothing inductor (choke) L_f, the more the pulse is pulled and its amplitude decreases due to inductance $X_L = \omega L_f$. The average current value also falls.

Typically, an smoothing inductor in half-wave circuits is not used, but used in double half-wave (Fig. 12.9).

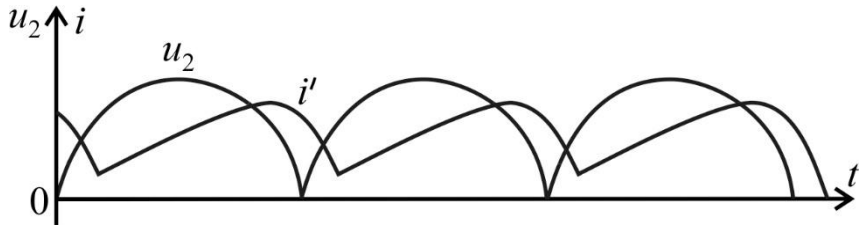


Figure 12.9

Varieties of smoothing filters (*LC-RC* filters; *L*-, *P*-, *T*- shaped) filters are shown in Figure 12.10, *a*, *b*, *c*.

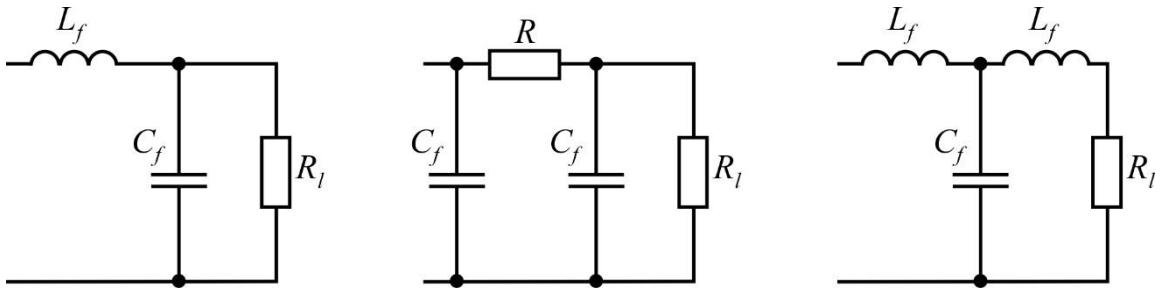


Figure 12.10

12.4.3. External characteristics of rectifiers. The load resistance R_l changes during operation, which causes a change in the load current I_l.

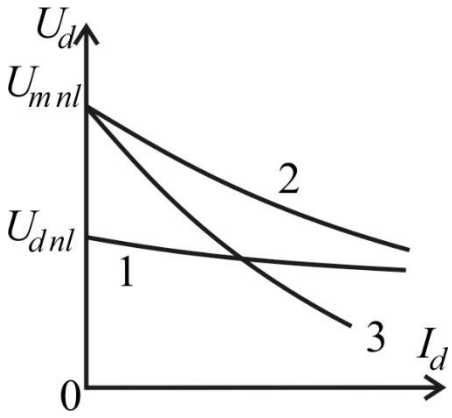


Figure 12.11

Transformers and valves (diodes) have certain values R_{tr} and R_f of resistances. At these resistances, the voltage drops from the current I_l, resulting in a change in the load voltage U_l.

External characteristic of the rectifier $U_l(I_l)$

$$U_l(I_l) = U_{nl} - (R_f + R_{tr})I_l = U_{nl} - R_f I_l - R_{tr} I_l,$$

where U_{nl} is the rectified voltage at $I_l = 0$;

$R_f I_l$ – the average value of the voltage drop across the diode resistance in the forward direction;

$R_{tr}I_l$ – the average value of the voltage drop across the resistance of the secondary winding of the transformer.

The external characteristic defines the boundaries of the change in the load current at which the rectified voltage does not decrease below the permissible value.

1 – a rectifier without a filter (characteristic is non-linear due to R_f);

2 – a rectifier with a capacitive filter;

In the no-load mode (I_l = 0), the rectified voltage is equal to the amplitude value $U_{m\,nl}$, and without a filter, to the average value.

For a half-wave rectifier – $U_{l\,nl} = \frac{U_m}{\pi} = 0{,}318U_m$;

For a double half-wave rectifier – $U_{l\,nl} = 2\frac{U_m}{\pi} = 0{,}636U_m$.

With an increase in the load current, curve 2 drops more sharply, since the drop also occurs due to a faster discharge of the capacitor to a lower resistance, which reduces the voltage on the load.

3 – rectifier with a *L*-shaped *RC* filter. An additional decrease in voltage is caused by a voltage drop across the series-connected resistor R_f.

12.5. Object of study

12.5.1. In Fig. 12.12 shows the schematic diagram of studies of a single-phase half-wave rectifier, which includes a rectifier diode *VD*1 and a load resistor *R*1. The circuit is connected to the terminals of the sinusoidal current source "~ 8V" of the bench power supply unit (**PSU**).

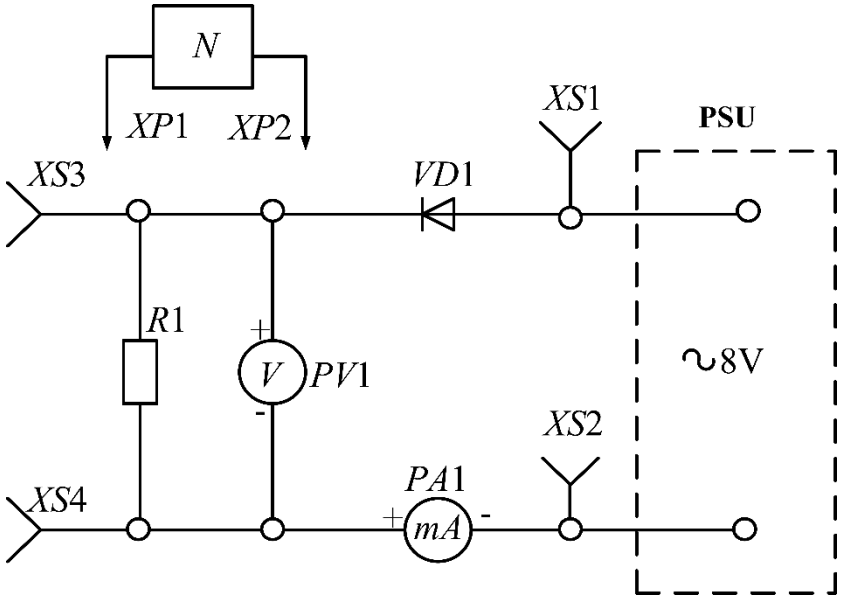


Figure 12.12– The schematic diagram for study of a single-phase half-wave rectifier

12.5.2. The three-point schematic diagram for conducting experimental studies of a single-phase double half-waved rectifier is shown in Fig. 12.13. The circuit is

assembled on the basis of transformer T and includes rectifier diodes VD1 and VD2 and resistor *R*2. The sinusoidal voltage to the circuit is supplied from the terminals "U_m" and "⊥" of the generator signal panel (**GSP)**.

12.5.3. The schematic diagram for carrying out experimental studies of a single-phase bridge double half-wave rectifier is shown in Fig. 12.14.

The rectifier unit VA includes a four-diode bridge circuit and has four terminals: inputs that connect to a ~ 8V sine wave power supply unit and outputs (+ and -).

A choke (smoothing inductor) *L* and capacitor *C* create a smoothing *LC*-filter and resistors *R*3 and *R*4 activate the rectifier's active load. One of the windings of the transformer T is used as a choke.

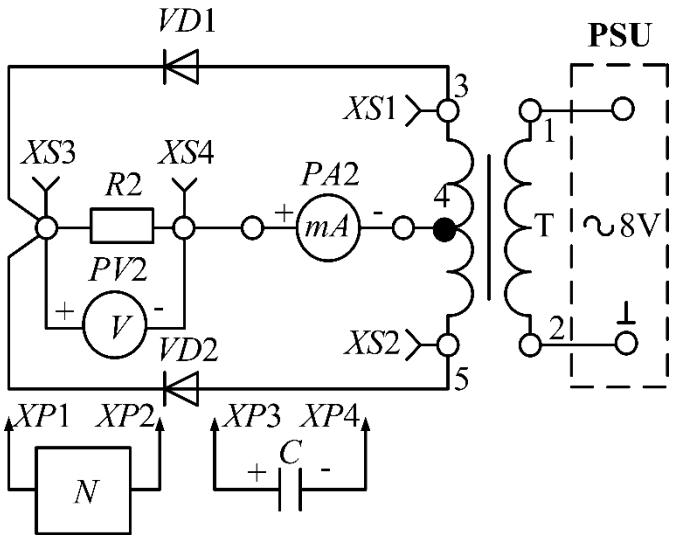


Figure 12.13 – The schematic diagram for study of a single-phase double half-wave rectifier with the lead of the midpoint of transformer

12.5.4. DC and voltage are measured respectively by milliammeters *PA*1, *PA*2 and voltmeters *PV*1, *PV*2. Using the N oscilloscope, in all circuits, the voltage form to the rectifier (sockets *XS*1, XS2) and after it (sockets *XS*3, XS4) is controlled.

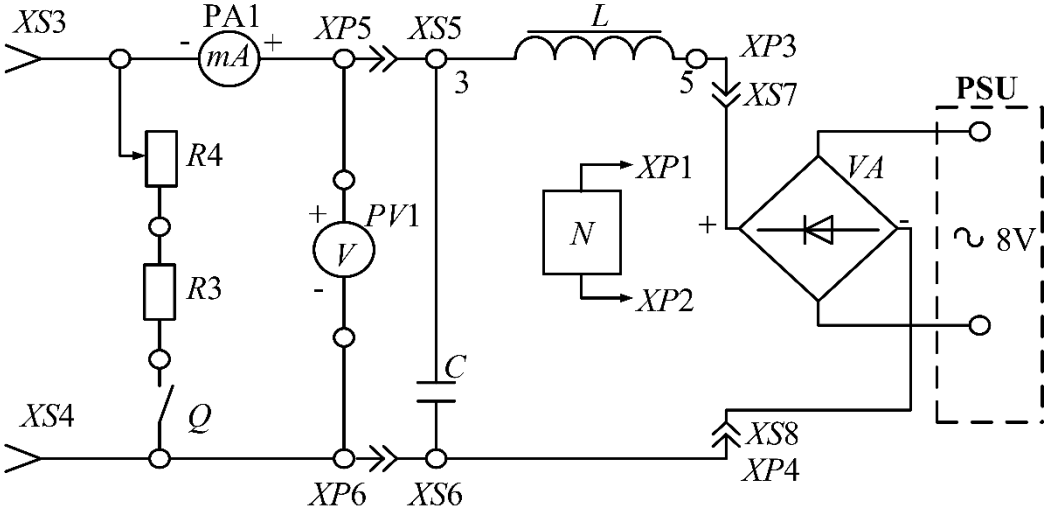


Figure 12.14 – A schematic diagram for study of a single-phase bridge double half-wave rectifier (Grets circuit)

The parameters of the elements included in the diagrams are given in Table 12.2 and Table 12.3.

Table 12.2

Diodes *VD*1, *VD*2	The rectifyer unit *VA*	Constant resistors			Variable resistor	Capacitor
КД209А	КЦ405Б	*R*1	*R*2	*R*3	*R*4	*C*
I_0 = 0,1 А	I_0 = 0,1 А	470 Ohm	1,5 kOhm	100 Ohm	470 Ohm	10 and 50 μF

Table 12.3

Oscilloscope	Milliammeter		Voltmeter		Switch	Transformer	Choke
N	*PA*1	*PA*2	*PV*1	*PV*2	*Q*	T	*L*
С1-67	50 mA	5 mA	15 V	5 V	MT1	-	T, clamps 3,5

12.6. The order of the experiment execution

12.6.1. Assemble the circuit according to Fig. 12.12 of the elements, the parameters of which are given in Table 12.2 and Table 12.3 for the study of a single-phase half-wave rectifier.

Turn on the **"Network On"** toggle switch on the **PSU**. Measure current and voltage and record voltage waveforms at the input and output of the rectifier. Disable network switch to **"Network Off"**.

Turn on the **"Network On"** toggle switch on the **PSU**. Measure current and voltage and record voltage waveforms at the input and output of the rectifier. Connect the 10 and 50 μF capacitors in parallel to the load resistor and again read the voltage waveforms across the load resistor. Disable the "**Network On**" switch.

12.6.2. Mount the cicuit according to Fig. 12.13 of the elements, the parameters of which are given in Table 12.2 and 12.3 for the study of the double half-wave rectifier with a midpoint output of a transformer. Set the waveform selector knob to the position "~ sine". Turn on the **GSP** switch and set the maximum signal voltage $\boldsymbol{U_m}$**/V** with the knobs. Measure current and voltage and draw voltage waveforms at the input and output of the rectifier. Connect the 10 and 50 μF capacitors in parallel to the load resistor and again read the voltage waveforms across the load resistor. Disable the "**GSP**-on" toggle switch.

12.6.3. Mount the diagram according to Fig. 12.14 for the study of a double half-wave bridge rectifier of the elements, the parameters of which are given in Table 12.2 and 12.3.

Turn on the **"Network On"** switch on the **PSU** and draw the voltage waveforms of the rectifier output if there is an *LC*- filter.

Read the external characteristic U_0 (I_0) of the filter rectifier. To do this, it is necessary to start from no-load mode, i.e. turn off the switch Q and measure the voltage U_0. Then turn it on and change the resistance of the resistor *R*4 from high to low. Record the measured values of voltage U_0 and current I_0 in Table 12.4.

Disable the **“Network On”** toggle switch.

Table 12.4

U_0, V						
I_0, mA	0					

Exclude the *LC*-filter from the diagram in Figure 12.14 (part of it between pins XP3, XP4 and sockets XS5, XS6) and insert pins XP5, XP6 into sockets XS7, XS8. Turn on the Network On toggle switch and repeat the experiments, i.e., draw the oscillation-diagrams of the rectifier output and read its external characteristic. Write the measured values of voltage U_0 and current I_0 in Table 12.5.

Disable the **“Network On”** toggle switch.

Table 12.5

U_0, V						
I_0, mA	0					

12.7. Processing the results of the experiment

1. To draw in one coordinate grid the external characteristics U_0 (I_0) of a two-period rectifier, both with and without the filter, using the data in Table 12.3 and 12.4, and analyze their differences.

2. Display and compare the waveforms of voltages of one- and two-period rectifiers and explain the reasons for the difference.

3. Display and compare the waveforms of a two-period rectifier without filter and filter, and explain the reasons for the difference.

Control Questions

1. Outline the schematic diagrams and explain the principle of operation of the rectifiers studied.

2. Display the time functions of the input voltage and the rectifier load, as well as any diode.

3. Specify the main electric parameters of the circuits of single-phase rectifiers. Compare different circuits on these parameters.

4. What are the parameters of the diodes for different rectifiers?

5. What is the purpose of filters? What filter in the circuits are used?

6. Explain why is a capacitor switched on in parallel with the load and a choke in series, and why they reduce the voltage ripple across the load?

7. What is the voltage or current ripple ratio?

Laboratory work 13

RESEARCH OF A LOW FREQUENCY AMPLIFIER

13.1. Purpose of the work

The purpose of the work is to study the principles of amplification of low-frequency electric signals and experimental study of a common emitter amplifier with a bipolar junction transistor, the read of the gain (amplitude) and amplitude-frequency characteristics (AFC) of this amplifier.

13.2. Theoretical provisions

An electronic amplifier is a device that provides an increase in the power of electric signals supplied to its input.

The amplifier includes:

1) an amplifying (active) element is a nonlinear element (transistor, electron lamp, etc.);

2) passive elements: resistive, capacitive, oscillatory circuit, etc .;

3) power supply (direct current, less often alternating current).

The source of input signals are: microphone, photocell, thermocouple, chemical current source, previous amplifier, etc.

Load of the amplifier can be: a resistor, an oscillating circuit, a transformer, an electric motor, a speaker, etc.

The purpose of the amplifier element is to convert the electric energy of the power source into the energy of amplified signals.

The simplest amplifier contains one active element with passive elements attached to it, and it is called an ***amplifier stage***.

13.2.1. The functional block diagram of the amplifier stage. The block diagram of an amplifier is shown in Fig. 13.1.

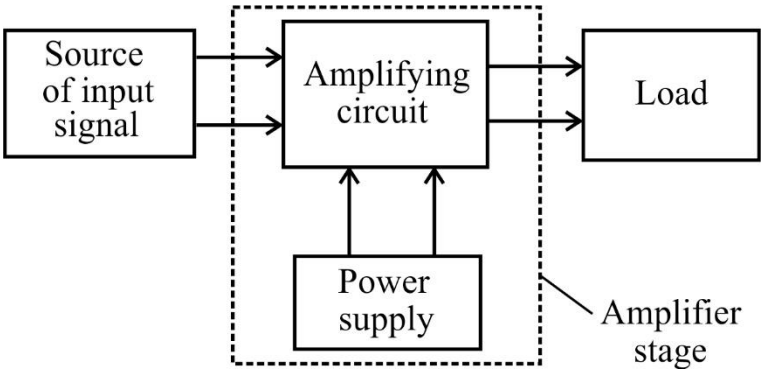


Figure 13.1 – The functional block diagram of an amplifier

The amplification process is to convert the energy of the power source into the energy of the output signal.

The input signal is a function of the input signal, and the power of the output signal due to the energy of the power source is much greater than the power of the input signal.

13.2.2. Amplifier classification.

By the nature of the amplified signals:

1) harmonic signal amplifiers; 2) pulse amplifiers.

By appointment:

3) voltage amplifiers; 4) current amplifiers; 5) power amplifiers.

By the nature of the amplifying elements:

6) transistor amplifiers (with bipolar junction transistors or field effect transistors);

7) tube amplifiers (electronic tubes); 8) magnetic amplifiers, etc.

According to the frequency range of electric signals:

9) amplifiers of low frequency; from tens of Hz to tens of kHz.

10) DC amplifiers; more precisely, amplifiers of slowly changing signals: from 0 Hz to tens and hundreds of kHz.

11) selective or selective amplifiers - amplifying signals in a very narrow frequency band. They are characterized by a small ratio of the upper to lower frequencies $f_h / f_l < 1{,}1$.

12) broadband amplifiers amplifying a very wide frequency band (from a few kHz to several MHz).

According to the type of interstage connections:

13) amplifiers with galvanic coupling;

14) amplifiers with resistive-capacitive coupling;

15) transformer coupled amplifiers;

16) amplifiers with communication through an oscillatory circuit.

13.2.3. Amplifier main features. *Gain* is the ratio of the signal at the output to the signal at the input of the amplifier.

We can distinguish between gains: voltage gain $\boxed{K_U = \frac{U_{out}}{U_{in}}}$;

current gain $\boxed{K_I = \frac{I_{out}}{I_{in}}}$;

power gain $\boxed{K_P = \frac{P_{out}}{P_{in}} = \frac{U_{out}}{U_{in}} \frac{I_{out}}{I_{in}} = K_U K_I}$.

These are dimensionless coefficients. There are very large values and this is inconvenient. Therefore, gain factors are used in logarithmic units – decibels (dB).

The relationship between dimensional and dimensionless coefficients is as follows:

$$\boxed{K_{P,\mathrm{dB}} = 10 \lg K_P} .$$

The values of the coefficients K_U or just K are tens ... hundreds. Sometimes this is not enough. Then a series connection of amplification stages is used.

Since $P \sim I^2$ or U^2, then $\boxed{K_{U,\text{dB}} = 20\lg K_U}$ $\boxed{K_{I,\text{dB}} = 20\lg K_I}$

$\boxed{K_U = 10^{\frac{K_{U,\text{dB}}}{20}}}$.

Reverse transition

If $K_{U,\text{ dB}} = 1$ dB, then $K_U = 10^{1/20} = 1{,}12$, i.e. gain of 12%.

The block diagram of a multistage amplifier is shown in Fig. 13.2.

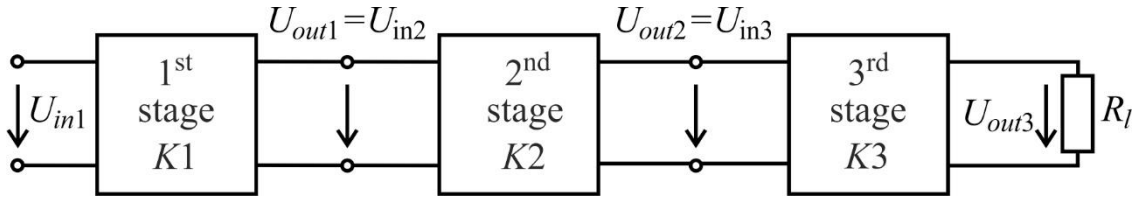


Figure 13.2 – Multi-stage amplifier

Total gain $K = K_1 \cdot K_2 \cdot K_3$ or $\boxed{K = \frac{U_{out3}}{U_{in1}} = \prod_{i=1}^{n} K_i}$.

Indeed $K = \frac{U_{out1}}{U_{in1}} \cdot \frac{U_{out2}}{U_{in2}} \cdot \frac{U_{out3}}{U_{in3}} = \frac{U_{out3}}{U_{in1}}$,

because $U_{out1} = U_{in2}$; $U_{out2} = U_{in3}$.

For dimensional coefficients

$$K_{\text{dB}} = K_{1,\text{dB}} + K_{2,\text{dB}} + K_{3,\text{dB}} = \sum_{i=1}^{n} K_{i,\text{dB}} .$$

Output power. With an active load, the output power of the amplifier

$$P_{out} = \frac{U_{out}^2}{R_l} = \frac{U_{m\,out}^2}{2R_l}$$

This is the net power developed by the amplifier in the load resistance. Its increase is limited by distortions due to the nonlinearity of the characteristics of the amplifying elements at large signal amplitudes.

The power at which the distortion does not exceed the allowable value is called the rated output power.

3. *Efficiency*

$$\boxed{\eta = \frac{P_{out}}{P_0} 100\%}$$

where P_0 is the power consumed by the amplifier from all power sources.

4. *Rated input voltage* – sensitivity. This is the voltage that must be brought to the input of the amplifier in order to obtain a given power output. Otherwise, there will be strong signal distortions.

5. *The range of amplified frequencies or bandwidth* – that region of frequencies in which the gain does not change more than is allowed by the technical conditions.

The expansion of the bandwidth leads to an increase in cost and complexity of the equipment.

13.2.4. A low frequency common emitter amplifier on a bipolar junction transistor. The transistor *VT* is *n-p-n* type in Fig.13.3. The polarity of the power supply E_{col} depends on this. Its value is usually taken 10 ... 15 V.

$$E_{CE} > U_{BE};\ \ I_{col} \approx I_{em};\quad R_{col} >> R_{em}, \text{ so}\quad U_{in} = I_{em}R_{em} << U_{out} = I_{col}R_{col}\ .$$

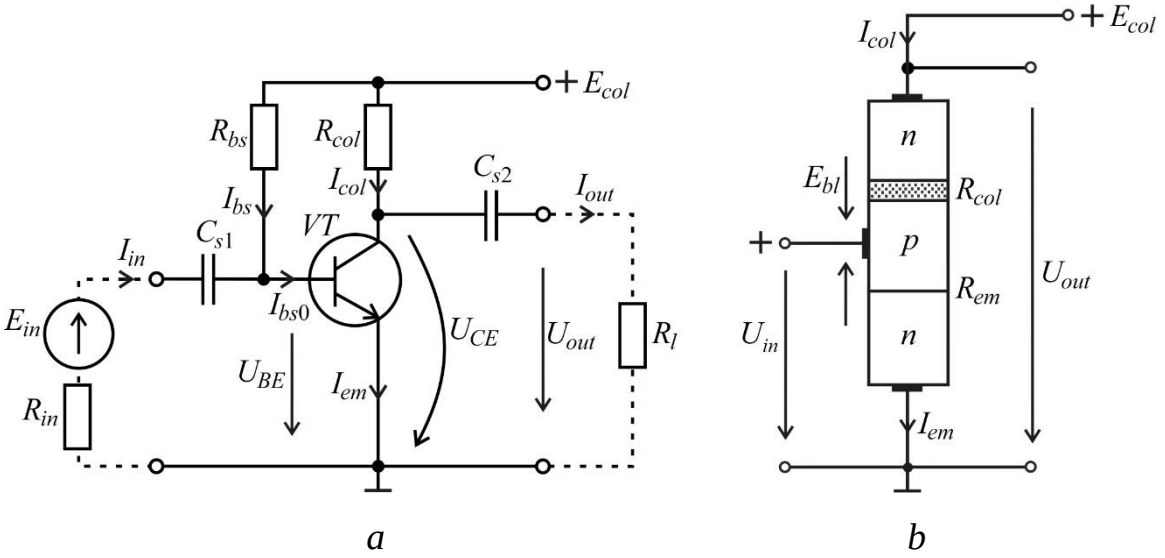


Figure 13.3 – A schematic diagram of a low frequency amplifier (*a*) and the structure of a *n-p-n* bipolar junction transistor (*b*)

The input signal arrives at the base and changes its potential relative to the grounded emitter. This leads to a change in the base current, and, consequently, to a change in the collector current and the voltage at the load resistance R_{col}.

The separation capacitor C_{s1} serves to prevent the DC component of the base current from flowing through the input signal source (without C_{s1}, the source will heat up and the transistor will change its operation mode).

Using a capacitor C_{s2}, an alternating voltage component U_{CE} is supplied to the output of the cascade, which varies according to the law of the input signal, but significantly exceeds it in magnitude.

The resistor R_b provides the choice of the initial operation point on the characteristics of the transistor and determines the mode of operation of the cascade of direct current.

For the collector circuit according to Kirchhoff's voltage law

$$E_{col} = U_{CE} + I_{col}R_{col}$$

I - U characteristic of R_{col}: $I_{col}(U_{CE})$ – linear,

I - U characteristic of *VT*: $I_{col}(U_{CE})$ – non-linear.

We build a load line $U_{CE} = E_{col} - I_{col} R_{col}$ for the resistor

We can build on two points:

1) $I_{col} = 0; \Rightarrow U_{CE} = E_{col}$; 2) $U_{CE} = 0 \Rightarrow I_{col} = E_{col} / R_{col}$.

For this and base currents I_b, you can find the current I_{col} and voltage U_{CE} (along the intersection of the curves). Fig. 13.4 shows the input and output characteristics of a bipolar junction transistor.

Using the resistor R_b, it is possible to obtain in the absence of an input signal a current I_{BE0} and a voltage U_{BE0} corresponding to the middle of the linear portion of the input characteristic (point A).

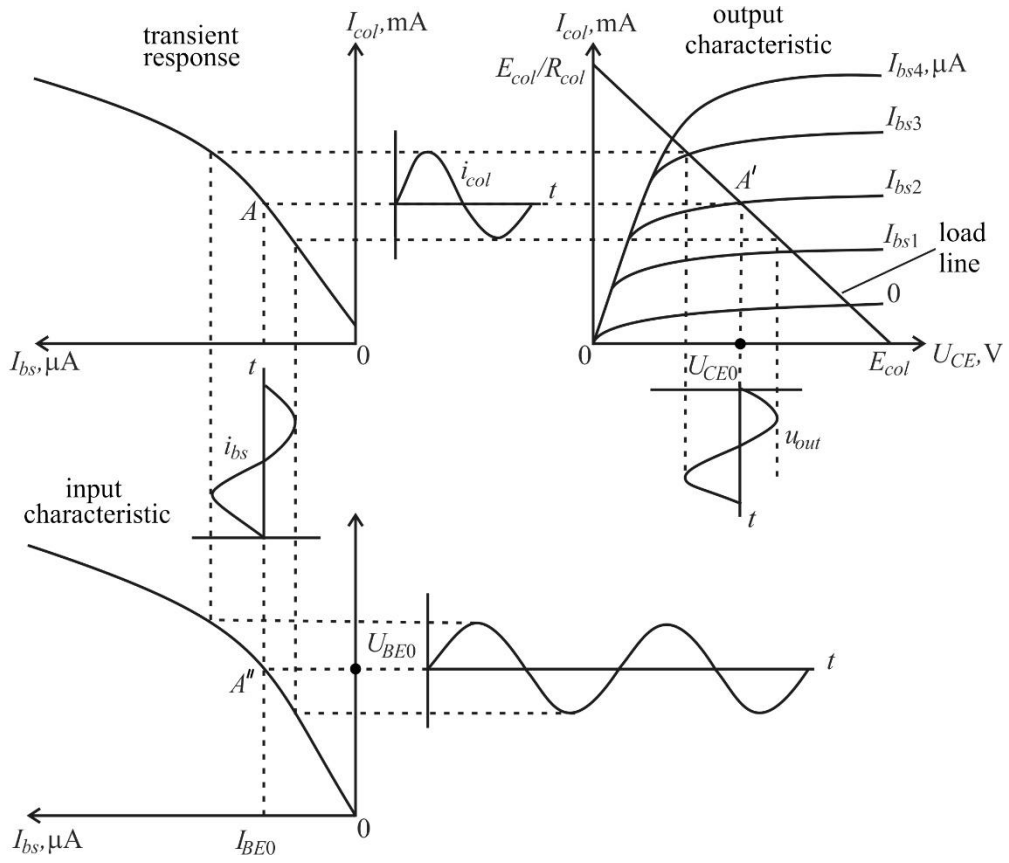


Figure 13.4 – Input and output characteristics of a bipolar junction transistor

The resistance of the resistor R_b is selected from the equation:

$$E_{col} = U_{BE0} + I_{BE0} R_b \quad - \text{at the no-load mode.}$$

$$R_b = \frac{E_{col} - U_{BE0}}{I_{BE0}}$$

The resistor R_b provides the bias current in the base circuit. Such a shift of the emitter junction is provided by a fixed base current. This is a fixed base current amplifier.

13.2.5. Amplifier temperature stabilization.

With increasing temperature, the current I_{col} increases due to an increase in minority charge carriers, which changes the characteristics of the transistor (the operation point shifts from point *A* in Fig. 13.4).

In this amplifier, the offset of the emitter junction is provided by a fixed base-emitter voltage, and the amplifier is called a fixed base voltage.

The no-load mode is ensured by the constant bias voltage of the emitter junction using the $R'_{bs} - R''_{bs}$ divider that is shown in Fig. 13.5.

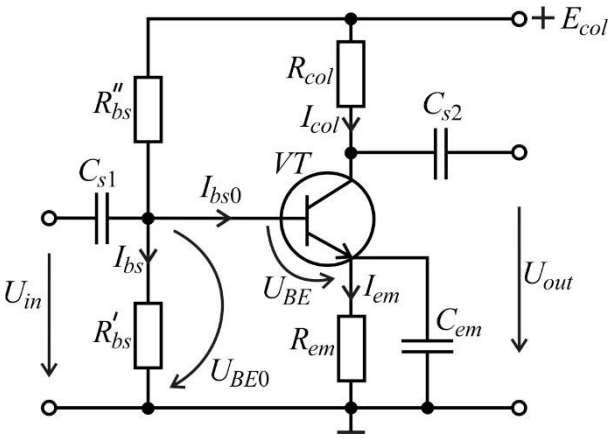


Figure 13.5 – Amplifier temperature stabilization

Voltage U_{BE0} (direct current in the absence of U_{in}):

$$U_{BE0} = I_{bs}R'_{bs} = \frac{E_{col}R'_{bs}}{R'_{bs} + R''_{bs}}$$ – an initial shift of the base.

According to Kirchhoff's voltage law:

$$U_{BE} = U_{BE0} - I_{em}R_{em} = \frac{E_{col}R'_{bs}}{R'_{bs} + R''_{bs}} - I_{em}R_{em} \quad .$$

In the presence of a resistor R_{em}, an increase in current $I_{em} = I_{b0} + I_{col}$ due to an increase in temperature leads to an increase in the voltage drop $I_{em}R_{em}$ on the resistor R_{em}, which causes a decrease in voltage U_{be}, and therefore currents I_{em} and I_{col}:

$$\boxed{T \uparrow \Rightarrow I_{col} \uparrow \Rightarrow I_{em} \uparrow \Rightarrow I_{em}R_{em} \uparrow \Rightarrow U_{BE} \downarrow \Rightarrow I_{bs} \downarrow \Rightarrow I_{col} \downarrow}$$

Thus, the resistor R_{em} plays the role of DC feedback.

For alternating current in the presence of U_{in}: the introduction of R_{em} creates a voltage drop $u_{em} = i_{em}R_{em}$, which reduces the amplified voltage.

Where i_{em} is the alternating component of the emitter current.

$$U_{BE} = U_{in} - i_{em}R_{em}.$$

To attenuate this negative phenomenon, C_{em} is set in parallel with R_{em}. The capacitance of C_{em} is such that $X_{em} = \frac{1}{\omega C_{em}} << R_{em}$ for all frequencies of the amplifier and then the amplified voltage is almost equal to the input

$$u_{BE} \approx u_{in} \ ,$$

So that we removed the feedback on alternating current.

13.2.6. Self-interference and distortion of the amplifier. The causes of interference at the amplifier output can be divided into 3 groups:

1) thermal noise;

2) noise of amplifying elements;

3) interference due to ripples in the supply voltage and interference from external electromagnetic fields.

The amount of total noise at the amplifier output should be significantly less than the signal voltage. Typically, the useful signal should exceed the interference level by at least 2 ... 3 times (by 6 ... 10 dB).

13.2.7. Amplitude response (Gain characteristic)

It is dependence $U_{\text{out}}(U_{\text{in}})$ shown in Fig. 13.6. At low voltage or in the absence of a signal input, the output voltage is determined by the level of intrinsic noise and the noise of the amplifier at $U_{in} < U_{in\min}$.

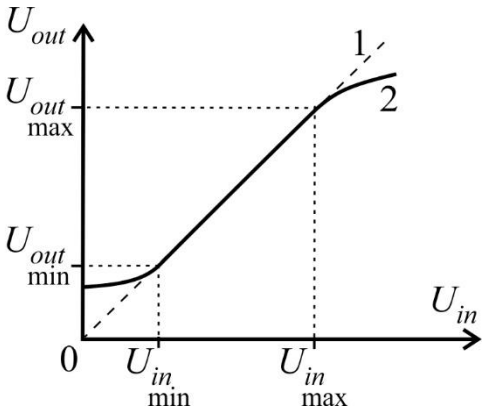


Figure 13.6 – Gain characteristic: 1 – ideal; 2 – real

At high input voltages $U_{in} > U_{in\max}$, the characteristic is distorted due to overload of the amplifying elements from the input side.

Estimated by the dynamic range of amplitudes in decibels

$$D_{dB} = 20 \lg \frac{U_{in\max}}{U_{in\min}}.$$

13.2.8. Amplifier distortion. Distortions can be: amplitude or nonlinear, frequency and phase.

Nonlinear distortion is a change in the shape of the curve of amplified oscillations caused by the nonlinear properties of the amplifier circuit (mainly due to the nonlinear characteristics of the transistor).

For example, how do nonlinear distortions appear in the input circuit of an amplifier due to a transistor? It is shown in Fig. 13.7.

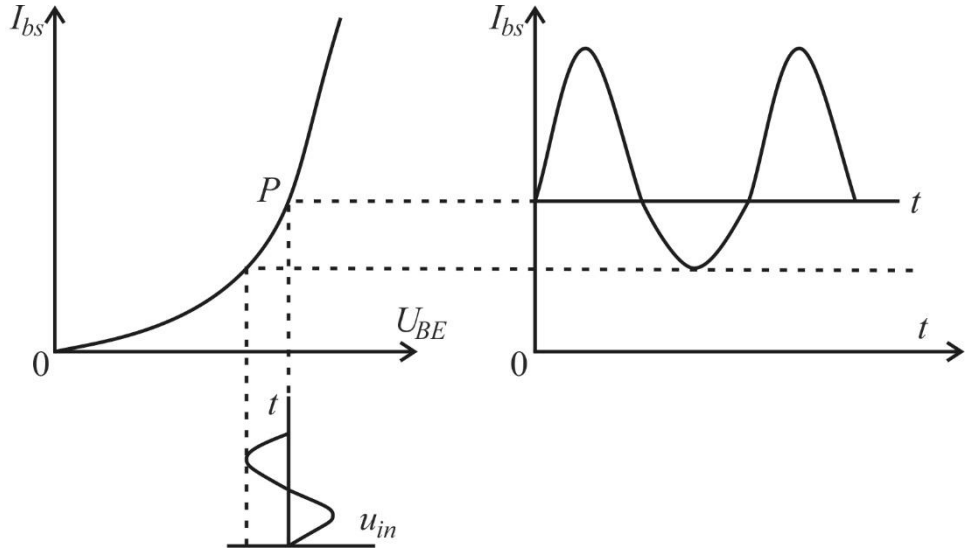


Figure 13.7 – Amplitude distortion

A sinusoidal signal is applied to the input of the amplifier. Getting on a non-linear section of the input characteristic of the transistor, this signal causes a change in the input current, the shape of which is not sinusoidal. This means that the output current and output voltage change their shape.

Frequency distortion is caused by a change in the magnitude of the gain at different frequencies. Reason is the presence of reactive elements in the amplifier (capacitors, inductors, mounting capacities, etc.).

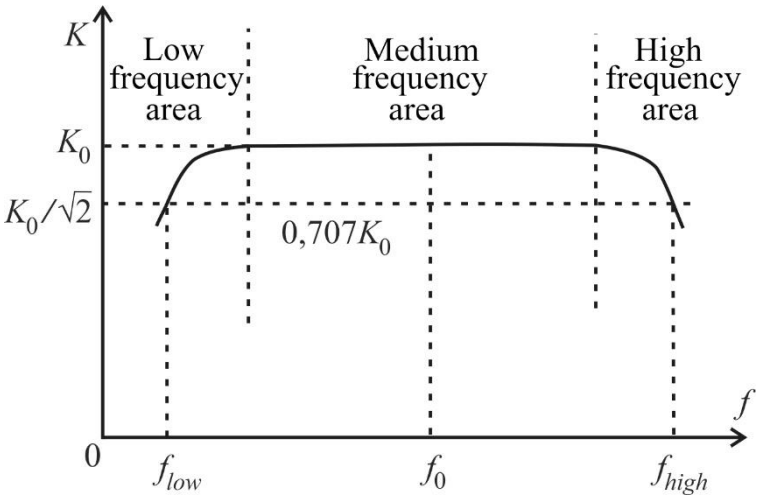


Figure 13.8 – Frequency distortion

Frequency distortion is estimated by the amplitude-frequency characteristic $K(f)$ or $U_{out}(f)$. It is shown in Fig. 13.8, where f_0 is the average transmission frequency; f_{low}, f_{high} are lower and upper boundary frequencies.

In the mid-frequency area or bandwith, the gain K is independent of frequency. The changes in the gain K are determined by the frequency distortion of the signal and are estimated by the frequency distortion coefficient

$$M(\omega) = \frac{K_0}{K(\omega)},$$

where $K(\omega)$ is the gain modulus at a certain frequency lying outside the mid-frequency region.

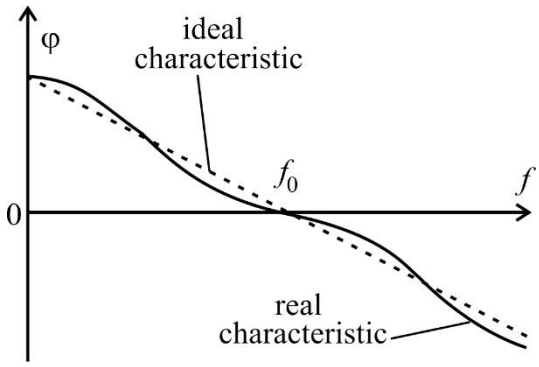


Figure 13.9 – Phase distortion

Phase distortion of the amplifier is estimated by its phase-frequency characteristic: the dependence of the phase angle φ between the input and output voltages of the amplifier on the frequency $\varphi(f)$ (Fig.13.9).

There is no phase distortion when the phase shift is linearly dependent on the frequency.

13.2.9. Types of feedback and their influence on amplifier parameters.

Feedback (*FB*) *is a transfer of a part of the energy of the amplified signal from the output circuit of an amplifier to the input circuit of the same amplifier.*

Block diagram of a feedback amplifier is shown in Fig. 13.10.

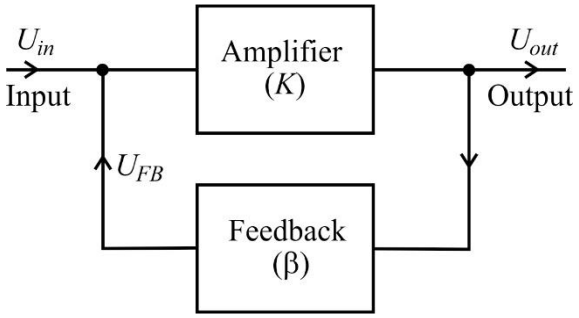


Figure 13.10 – Feedback in amplifiers

The feedback circuit is characterized by a transmission coefficient or feedback coefficient β, showing how much of the output signal is transmitted to the input of the amplifier

$$\beta = \frac{U_{FB}}{U_{out}} \ .$$

Usually $|\beta| < 1$.

If the voltage at the feedback output U_{FB} is in counter-phase to the input U_{in}, then such feedback is called negative.

If the voltage at the feedback output U_{FB} is in phase to the input U_{in}, then such feedback is called positive (it is used in oscillators to maintain oscillations).

Types of feedback:

1) internal *FB* – arises due to the physical properties of amplifying elements;

2) parasitic *FB*– arises due to parasitic capacitive and inductive connections between the input and output circuits;

3) artificial *FB* – it is specially created to reduce non-linear distortions, stabilize the position of the operation point, etc.

Various types of feedback are shown in Fig. 13.11:

4) input feedback; 5) output feedback; 6) voltage feedback;
7) current feedback; 8) series feedback; 9) parallel feedback.

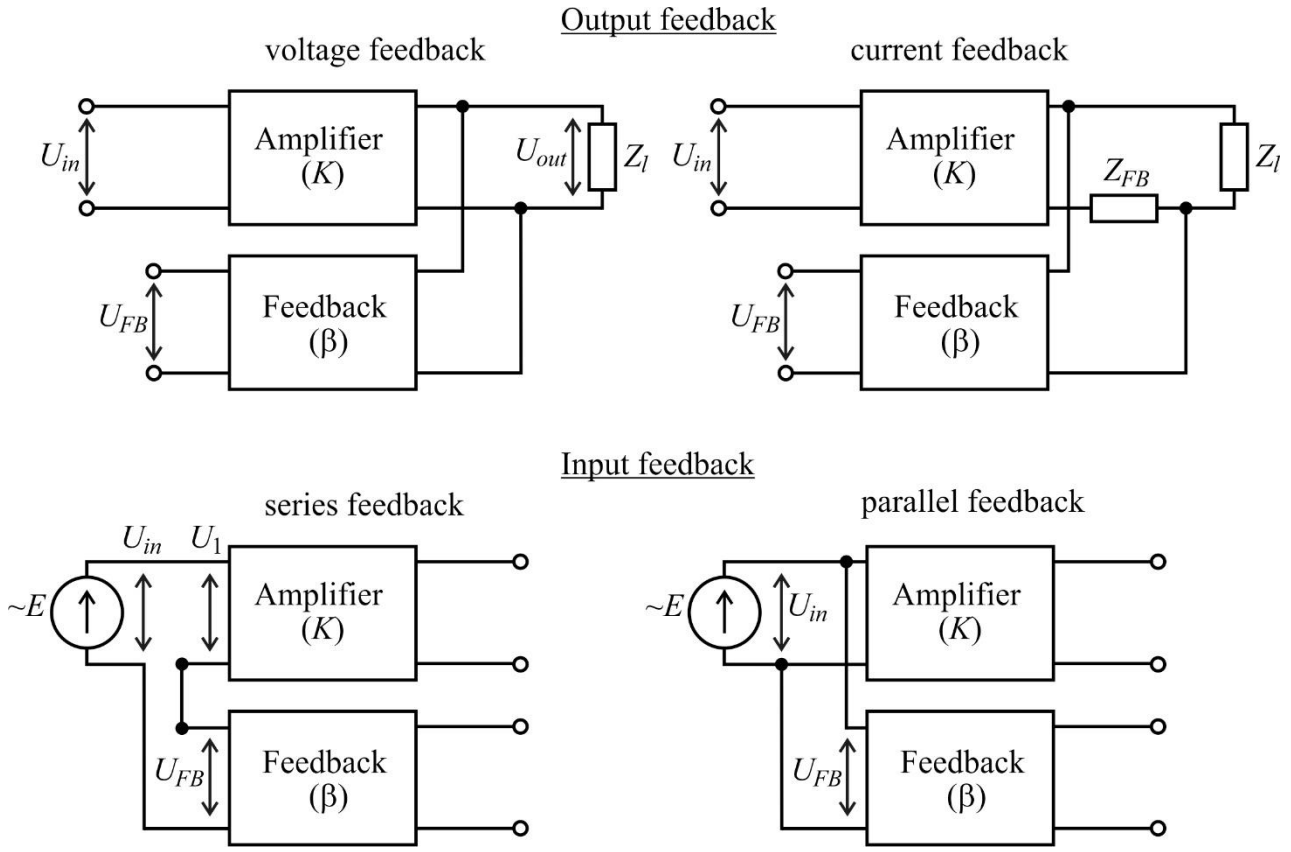


Figure 13.11 – Types of feedback in amplifiers

Consider the negative series feedback which is shown in Fig.13.12.

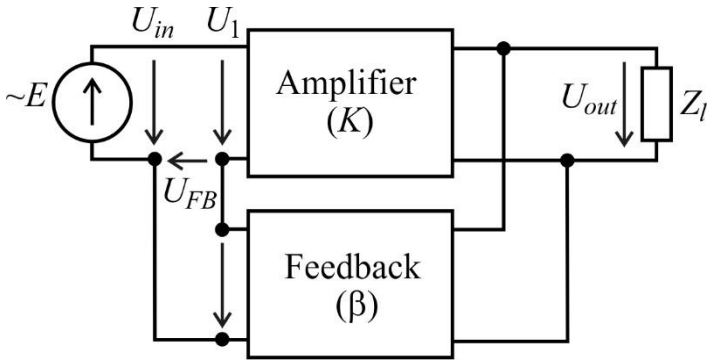


Figure 13.12 – Feedback influence on gain

Feedback voltage is applied to the input circuit of the amplifier

$$U_{\text{FB}} = \beta U_{out}, \quad \text{because} \quad \beta = \frac{U_{\text{FB}}}{U_{out}}.$$

$$U_1 = U_{in} - U_{\text{FB}} = U_{in} - \beta U_{out},$$

whence we obtain : $U_{in} = U_1 + \beta U_{out}$.

Without feedback $K = \frac{U_{out}}{U_{in}} = \frac{U_{out}}{U_1}$.

In the presence of negative feedback (NFb):

$$K_{\text{NFb}} = \frac{U_{out}}{U_{in}} = \frac{U_{out}}{U_1 + \beta U_{out}} \cdot \frac{1}{U_1} = \frac{\frac{U_{out}}{U_1}}{\frac{U_1}{U_1} + \beta \frac{U_{out}}{U_1}} = \frac{K}{1 + \beta K};$$

$$\boxed{\text{K}_{\text{NFb}} = \frac{K}{1 + \beta K}}.$$

Thus, the NFb reduces the gain by a factor of one $(1 + \beta K)$.

The value $(1 + \beta K)$ is called the NFb depth.

Using of negative feedback:

1) increases the stability of the gain *K* of the amplifier when changing the mode of the amplifier element (frequency, temperature, signal amplitude, etc.);

2) extends the bandwidth, reduces the level of nonlinear distortion, background and noise. The frequency response is smoothed (Fig. 13.13);

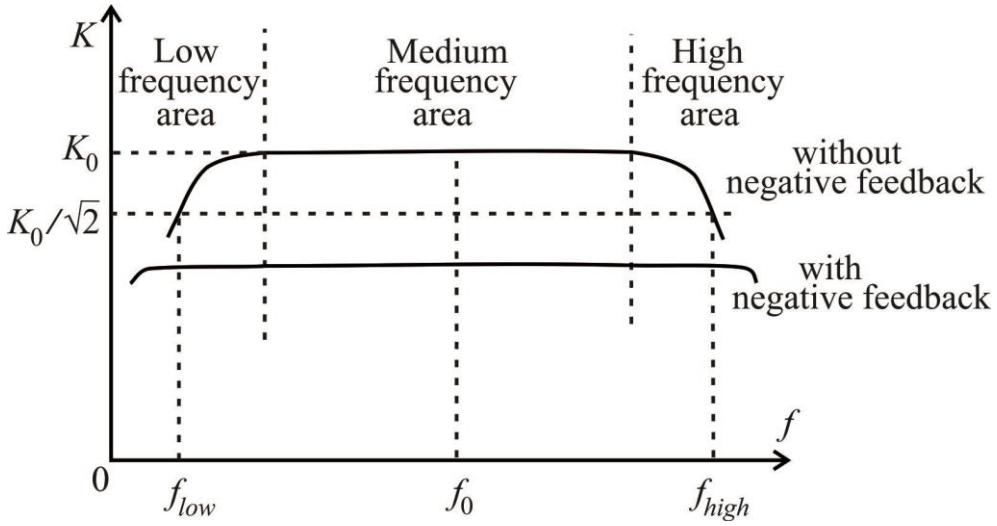


Figure 13.13 – Negative feedback influence

3) it is possible to reduce or increase the input and output resistances, for example, when matching loads, amplifying stages, etc.

$$Z_{in} = \frac{U_{in}}{I_{in}}; \qquad Z_{out} = \frac{U_{out}}{I_{out}}; .$$

With positive feedback (PFb), the gain increases:

$$\boxed{K_{\text{PFb}} = \frac{K}{1 - \beta K}}.$$

If $\beta K \approx 1$, then $K_{PFb} \to \infty$, i.e. the amplifier self-excites and begins to work as an oscillator.

13.3. Object of study

The object of research is a low-frequency amplifier (LFA) with a resistive-coupling link, the circuit of which is shown in Fig. 13.14. It includes a bipolar junction transistor *VT*, a collector resistor *R*3, resistors *R*1 and *R*2 of the voltage divider, which provides a direct voltage offset of the operating point at input voltage-current characteristics of the transistor. The circuit also contains the load resistor of the amplifier *R*5, the capacitors *C*1 and *C*2. The resistor *R*4 and the capacitor *C*3, which are connected in parallel, create a circuit of thermal stabilization of the operation mode of the amplifier.

The direct voltage on the amplifier is supplied from the terminals "+15 V" and "0" of the power supply unit (PSU) of the bench, and the voltage of the input signal is from the terminals "$\boldsymbol{U}_m$" and "⊥" of the signal generator (GSP), which is also contained on the bench. This generator must be switched on to the sine waveform "~". The DC voltage is measured by a *PV* voltmeter placed on the bench's power supply units, the voltage and frequency of the amplifier signals are measured by an oscilloscope, which is switched on using the *XP*1 and *XP*2 pins alternately to the sockets *XS*1, *XS*2 at the input and *XS*3, *XS*4 at the output.

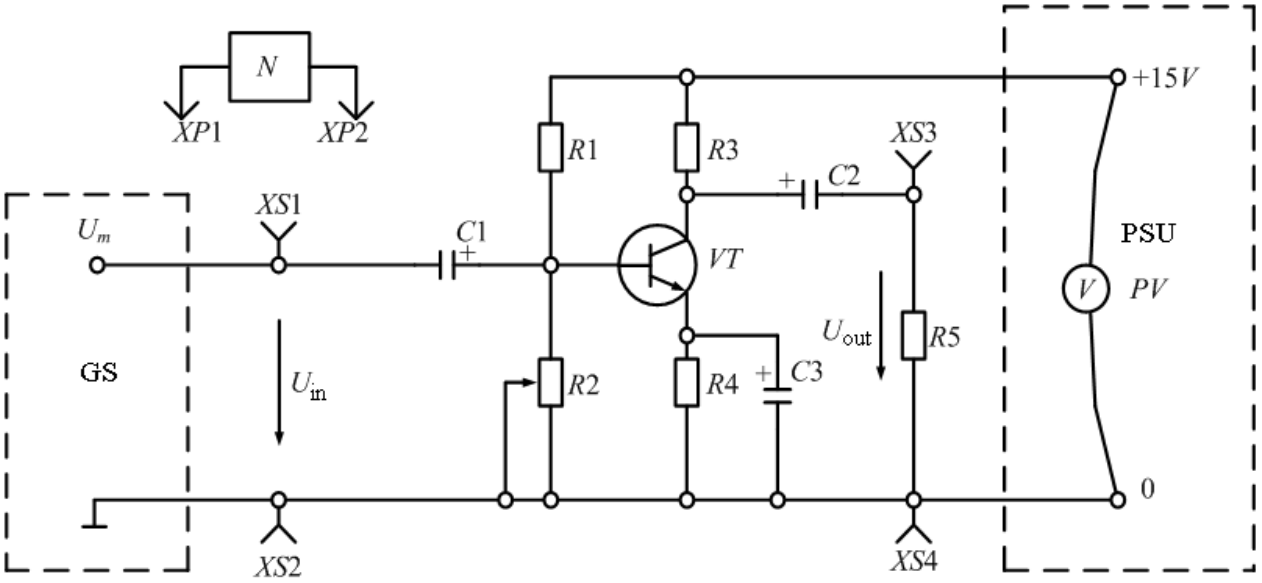


Figure 13.14 – A schematic diagram of a low-frequency amplifier

The parameters of the elements from which the circuit is mounted are given in Table 13.1.

Table 13.1

*R*1, kOhm	*R*2, kOhm	*R*3, kOhm	*R*4, kOhm	*R*5, kOhm	*C*1, μF	*C*2, μF	*C*3, μF	*V*1
47	150	10	680	22	10	10	50	KT315A

13.3. The order of the experiment execution

13.3.1. Assemble the circuit according Fig. 13.14 from the elements in Table 13.1, connect the oscilloscope to the input of the amplifier and carry out its adjustment. Switch on the power supply and set the amplifier to 15 V, measuring it with a PV voltmeter. Turn on the signal generator.

13.3.2. Obtain the amplitude characteristic of the amplifier $U_{\text{m.out}}$ ($U_{\text{m.in}}$) at the frequency $f = 1000$ Hz.

To read the amplitude characteristic, it is necessary to set a certain time f of the signal on the generator, check it with an oscilloscope, switch the oscilloscope to the output of the amplifier and adjust the resistor $R1$ and the signal amplitude knob of the generator "U_m/V" to achieve the maximum magnitude of non-sinusoidal amplifier output. Measure the signal amplitudes at the output of the $U_{m.\text{out}}$ and the input of the $U_{m.\text{in}}$ the amplifier using an oscilloscope. Further, by modifying the input signal, continue measuring the input and output signals. The results of measurements are recorded in Table 13.2. Measure till output signal will not disappear.

Table 13.2 Amplitude characteristic $f = 1000$ Hz = const;

$U_{m.\text{in}}$, mV	0					
$U_{m.\text{out}}$, V						

13.3.3. To read the amplitude-frequency characteristic $U_{m.\text{out}}(f)$ at the amplitude of the input signal $U_{m.\text{in}}$, equal to 0,5 $U_{\text{m.x, max}}$, where $U_{\text{m.NL, max}}$ – the largest amplitude, which was measured at a frequency of 1000 Hz in the previous experiment. Keeping the amplitude of the input signal further unchanged, it is only necessary to change its frequency f from 20 to 20000 Hz (the indicative values are in Table 13.3) and to measure the amplitude of the signal U_m.with the output of the amplifier. The experiment data should be entered in Table 13.3.

Table 13.3 Amplitude-frequency characteristic $U_{m.\text{in}}$ = _____mV;

f, Hz	20	40	100	200	1000	2000	10000	20000
$U_{m.\text{out}}$, V								
K_U								
ln f								

13.4. Processing the results of the experiment

13.4.1. According to Table 13.2 to draw the amplitude characteristics $U_{m.\text{out}}(U_{m.\text{in}})$ for each of the frequencies f.

13.4.2. According to Table 13.3 to calculate the gain of the amplifier

$K_U = U_{m.out} / U_{m.in}$ and build an amplitude-frequency characteristic in the form of a more obvious dependence $K_U(\ln f)$, than addiction $U_{m.out}(f)$. Analyze the behavior of this characteristic.

Control Questions

1. Explain the operating principle of the amplifier, using the volt-ampere characteristics of the transistor.

2. Explain the purpose of individual elements in the amplifier structure.

3. Explain the causes of the nonlinearity of the amplitude characteristic.

4. Explain the reasons for “blockage” of the amplitude-frequency characteristic of the amplifier at low and high frequencies.

5. What is the purpose of negative feedback?

6. Why does the amplifier’s operation depend on the temperature regime and how does this dependence decrease?

L a b o r a t o r y w o r k 14

MICROPROCESSOR SYSTEM RESEARCH

14.1. Purpose of the work

The purpose of the work is to consolidate theoretical knowledge about the structure of the microprocessor system and the principles of its operation.

The tasks of the lesson are to acquire the skills of working with a microprocessor system.

14.2. General theoretical provisions and information about microprocessors

Microprocessors (MP) are devices that perform the functions of software processing of information, including its input and output, decision-making, arithmetic and logical operations, and they are implemented using the technology of microcircuits of a large degree of integration. A microprocessor system is a small computer (electronic computing machine), in which four main devices can be distinguished: arithmetic-logic, control, memory, and an information input-output device, which is usually called a peripheral device (Fig. 14.1).

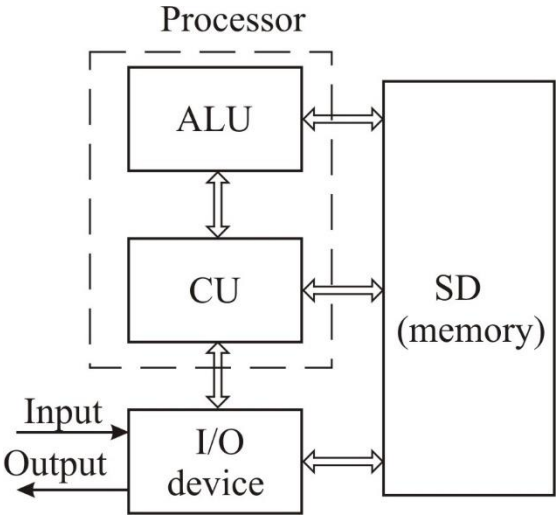


Figure 14.1 – A functional diagram of a microprocessor system

Arithmetic-logical unit (ALU) is used to perform arithmetic and logical operations on numbers represented in binary code.

The control unit (CU) controls the operation of the ALU and other devices of the microprocessor system according to special commands, the order of execution of which is determined by the given program.

A storage device (SD), or memory, is intended for storing processing programs and information (data) that is processed.

Input-output devices (I/O) of information, or peripheral devices, are used to bring the input information to the form required for input into the microprocessor

system and the output of the results of information processing in the proper form, for example, a sequence of numbers, tables, graphs.

ALUs closely interacting with CU, create a single whole – the central processor, or processor for short (from the English to process – to calculate). Thus, the processor is a device designed for automatic processing of information according to a given program.

Modern integrated technology makes it possible to perform processor elements in the form of one or several large integrated circuits. Such processors are called microprocessors.

By purpose, MPs are divided into universal (general purpose) and specialized. Universal MPs are used to solve various problems and are part of general-purpose computers. Specialized MPs are used to solve a specific problem according to a defined program. A microprocessor, permanent (ROM) and operational (RAM) memory devices compatible with it, as well as a large integrated circuit of auxiliary assignment, which ensures the conjugation of MP with ROM, RAM and I/O, create a microprocessor kit. According to the structural feature, MPs are divided into single-crystal and multi-crystal. In a multi-crystal MP, its constituent parts are located in different crystals based on the functions they perform and on the basis of their capacity. In single-crystal MPs, all components of the microprocessor are made in one crystal. In a microcomputer, in one semiconductor crystal, in addition to the MP, there are a clock pulse generator (timer), a I/O control device, small RAMs and ROMs.

Each MP operates with words, which are a sequence of symbols of a certain length: 4, 8, 16 and 32 bits, or digits. A group of bits that can be processed by a computer in one operation step creates a machine word. The length of a machine word is determined by the number of bits in one computer memory register.

For microprocessor technology, one of the main concepts is a byte – an eight-mbit word used to exchange digital information between nodes of a microprocessor system. In bytes, the length of words and the capacity of the storage device are expressed.

14.2.1. **Microprocessor structure**. The microprocessor contains three main nodes: ALU, CU and a node of registers (Fig. 14.2). An internal data bus is used to communicate between these nodes. It consists of eight lines (for an eight-bit MP), which transmit 8-bit words (bytes) and command information. The transmission of words on the internal data bus is carried out in both directions, but in different time intervals that do not overlap.

The main part, or the core of the MP, is the ALU, which performs data processing. Typical ALU operations: addition, subtraction, logical addition (OR), logical multiplication (AND), addition modulo 2 (EXCLUSIVE “OR”), inversion, shift, transfer. Usually, the ALU has two inputs, called input ports, and one output, or output port.

Data to the input ports of the ALU comes from the internal data bus or from a special register called the accumulator, through buffer registers, or registers of operands, intended for temporary data storage.

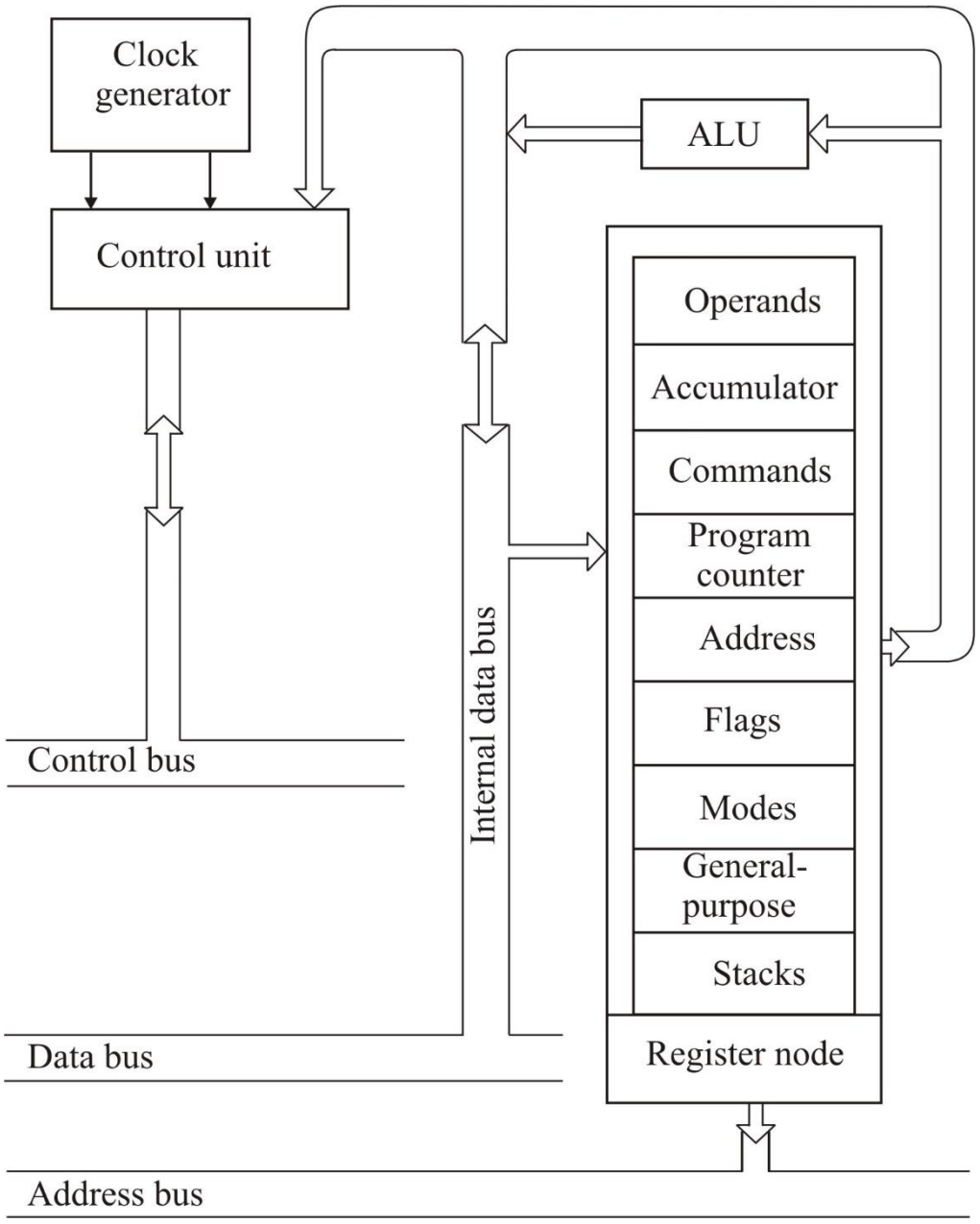


Figure 14.2 – The structure of a microprocessor

The buffer register through which data from the accumulator is received at the ALU input is called the accumulator buffer. The result obtained during the operation from the output port of the ALU enters the accumulator, which is also called the accumulating register. The battery buffer eliminates the situation in which the input and output of the ALU are connected to the battery at the same time.

The operation of the ALU and internal registers is managed by the CU, which extracts the next command from the command register, deciphers it, that is,

determines which operation should be performed, and ensures the execution of this operation in the ALU.

The order of arrival of the commands necessary to solve the problem is ensured by a register called the command counter. The command counter can have more digits than the length of the data word. For example, in 8-bit MPs with a memory volume of 64 K = 65536 words, a 16-bit command counter is used. As a result, you can write a command to any memory cell.

Before executing the program, a number is written into the command counter, which determines the address of the first program stored in the memory. This number from the instruction counter is then written into the 16-bit memory address register. The address of a new command is sent from the memory address register to the memory control device via the address bus. At the indicated address, the first command is read from the control panel, which is written into the command register. The considered cycle of operations is called the sampling cycle or the addressing phase. After recording the command in the register, the CU performs its recognition (decoding), and the ALU receives signals that stimulate the execution of this command. This process is called a cycle or command execution phase. The fetch loop together with the command execution loop forms the command loop. At the start of a command execution cycle, the command counter is automatically incremented by one, and it adjusts to the next command. Therefore, during the execution of a command, the command counter contains the address of the next command.

The sign register, or flag register, is used to indicate various signs of the results of operations performed by ALU: zero result, overflow, etc. It consists of separate triggers, called flags, which, depending on the manifestation of one or another symptom, are set to the state "0" or "1".

The status register receives information from the sign register and, depending on the sign values, allows you to change the sequence of command execution and perform so-called conditional transitions. At the same time, the content of the command counter changes, and it is adjusted to sample not the next, but the proper command. In this way, the presence of conditional transition commands makes MP more universal, allows you to choose different ways of solving the problem depending on the conditions that arise during the solution.

General-purpose registers are used as storage devices for intermediate results of calculations, addresses and commands, and sometimes as accumulators. The number of such registers in MP can reach up to 16, and their bit rate can be different. Separate general-purpose registers can be connected to each other in series and treated as one register with a large number of digits.

Stack registers are divided into stack registers and stack pointer. These registers allow you to organize the necessary sequence of command execution without exchanging with the control unit. The stack registers are connected in such a way that the first command written in the first register is "pushed" into the second register when the second command is written, and the second command is written in the first register. When writing the third command, the first goes to the third register,

the second to the second, and so on. When selecting commands from the stack, the last one is selected first, then the penultimate, etc., just as the last piece of wood (from the English stack - stack) is taken first from a stack of firewood.

The number of registers (depth) of the stack is an important characteristic of MP. To increase the depth of the stack, it is often organized in some area of the external SD.

The stack pointer specifies the address of the stack cell (register) filled by the last instruction. This cell is called the top of the stack. After selecting a command from the stack, the content of the stack pointer is decremented by one, and when the next command is written to the stack, it is increased by one.

The highly stable clock pulse generator ensures interaction and coordination of the work of all nodes of the microprocessor system. With the help of clock pulses, machine cycles and command cycles are formed. The machine cycle is the time required to retrieve one byte of information from memory or execute a command defined by one machine word.

14.2.2. Microprocessor command system. The microprocessor system must receive information from the outside, process it and send the results in the opposite direction. It performs operations according to specified inputs called commands. The sequence of commands makes up the program, and the set of commands known to the MP creates its command system.

A command, like data, is represented in binary code, creating a machine word. The length of the command word can be equal to one, two or more bytes, that is, it can contain 8, 16 or more bits. Each command must contain certain information and determine: 1) the type of action to be performed (the part of the command that defines this operation is called the operation code ; 2) data source (this information is contained in the data address field: addresses of operand 1 and operand 2); 3) address of the result; 4) the address of the next command. The generalized structural diagram of the MP command is presented in Fig. 14.3.

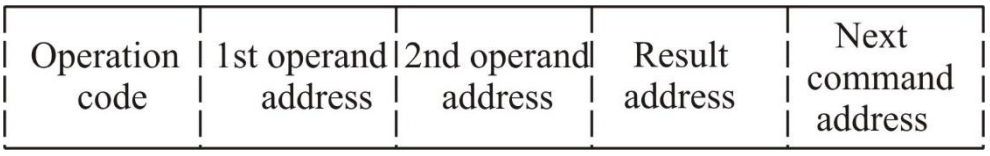


Figure 14.3 – Generalized structural diagram of the MP command

Thus, two main parts can be distinguished in the command – the CPC and the address. The operation code sets the MP to perform the desired operation, and the address indicates the location of the data operands involved in the operation.

In modern computer systems, single-address commands (16-bit) are most often used, containing the code and the address of one operand. If two operands are involved in the operation, then the address of the second operand is considered known. Such an address is most often an accumulator, in which the second operand is sent before the start of the operation. The result of the operation is also placed at a fixed address, usually at the location address of the second operand.

Commands that implement a given program are entered into a specified part of the software through an input-output device.

The set of commands executed by MP is divided into a number of groups, the main ones of which are commands for arithmetic and logical operations, transfers, input-output, control, access to routines, and some special commands.

Commands of arithmetic and logical operations ensure the execution of operations of arithmetic addition, subtraction and multiplication of binary and binary-decimal numbers, their comparison, as well as the execution of operations of logical addition, logical multiplication, addition by modulo (EXCLUSIVE “OR”), inversion of numbers, i.e. replacing zeros with ones, and ones with zeros, etc. After executing these commands, the result of the operation is sent to the accumulator or to the SD cell specified in these commands.

Transfer commands are used to transfer data from one memory cell to another, to the battery or vice versa. As a rule, these commands are executed without destroying the data in the original cells, that is, after executing the forwarding command, the same data is found in the original and in the re-specified memory cells. Transfer commands include commands for loading a register, a register pair, and an accumulator, transferring from a register to a register, and writing the contents of the accumulator to memory.

Input-output commands are used to enter through the data bus input information, presented in binary code, into the MP battery or to output the contents of the battery to the information display device. Input or output of information is carried out according to the commands "Input" or "Output".

Control commands include unconditional and conditional transition commands. These commands change the contents of the command counter and break the sequence of execution of program commands. With an unconditional transition, a violation of the program execution sequence occurs every time the program is executed. At the same time, the address of the cell in which the command is stored and to which the transition is carried out is contained in the address part of the command to which this transition is carried out.

With conditional transitions, the sequence of execution of program commands is broken only if the results of calculations provided by the program satisfy some set condition.

Subroutine access commands are types of control commands. Usually, routines are stored in stack registers, which, in most cases, are placed in the program. Writing information to the stack is called loading data into the stack, and retrieving it from the stack is called removing data from the stack.

When calling the subroutine, the current content of the command counter is first filled. Then the address of the first subroutine command is written into the counter. The last command of the subroutine is the “Return from subroutine” command, after which the number corresponding to the interrupted command of the main program is restored in the counter. The "Return from subroutine" command can also be used to switch from one subroutine to another if subroutine nesting is used.

A special form of a subroutine is an operation called an interrupt. It consists in the fact that the termination of the actions of the current program is carried out arbitrarily at the request of an external control signal. Since the current program can be interrupted anywhere, it is necessary to ensure the normal operation of the MP after returning from the interruption. For this, at the initial moment when the interrupt command is received, the contents of the accumulator registers, sign registers, and stack states are memorized.

Special commands include interrupt enable, interrupt disable, stop, and idle operation commands. When executing the "Non-working operation" command, no operations are performed, and the content of the address counter is increased by one, after which the next command is executed.

14.2.3. General concepts about microcomputers. Microcomputers are primarily intended to replace specialized logic circuits and are used as a component of various information and control systems.

Currently, the following types of microcomputers can be distinguished, on the basis of which it is possible to build multi-machine and multi-microprocessor computing systems:

- controllers are built-in microcomputers. They are used to solve local objects control problems and can be used as controllers of devices connected to a large computer or as control machines of lower control circuits;

- controlling microcomputers. Designed for the construction of control systems for sufficiently complex objects or processes: technological lines, measurement complexes, etc.;

- computational engineering microcomputers. They are intended for individual use. External devices of such a computer can be built into the body of the machine, and their set includes devices that are minimally necessary for computing and data processing: a digital, alphanumeric and functional keyboard, an alphanumeric indicator, a printing device, an external memory device.

The appearance of microprocessor sets of large integrated circuits led to the appearance of fundamentally new directions in the application of digital computing technology and allowed for embedded control, distributed control, distributed computing.

Calculators are one of the types of microcomputers. The microprocessor as a device with a high degree of integration from the point of view of technology is the result of the improvement of the calculator made on a separate crystal. Some large integrated circuits, called microprocessors, are designed primarily for calculators. Calculators are divided into simple and programmable.

Simple calculators are intended for carrying out the simplest calculations (Fig. 14.4). They can process, given the small information capacity of the memory device, only a limited set of numbers.

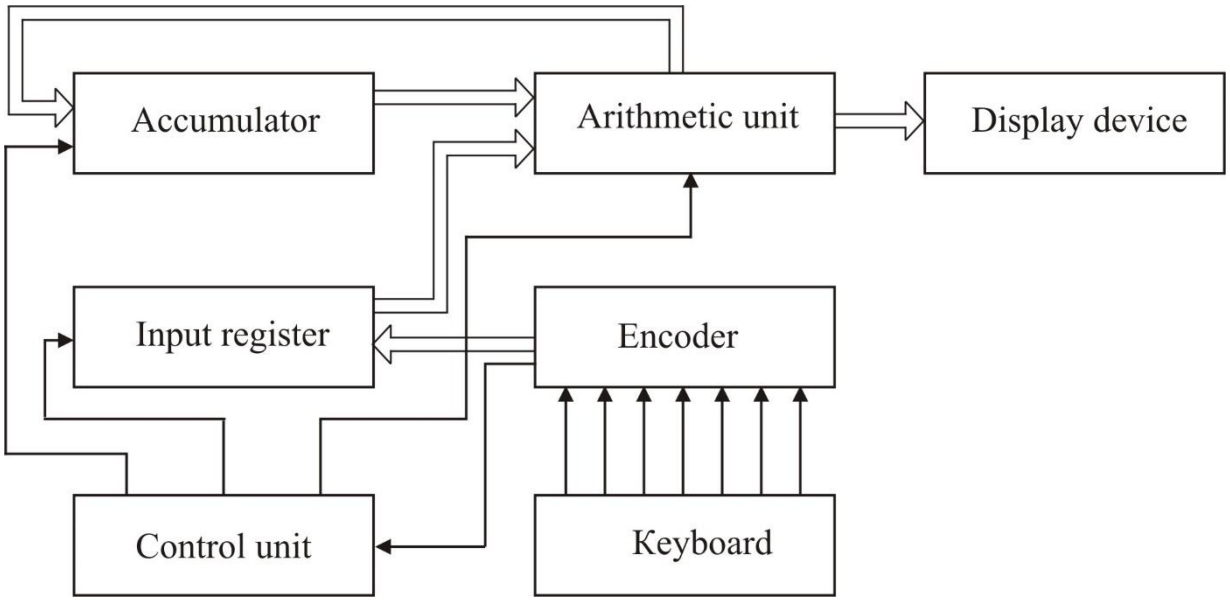


Figure 14.4 – A functional diagram of a non-programmable (simple) calculator

A non-programmable simple calculator contains two registers: input and accumulator. Arithmetic operations are performed in the arithmetic device on the numbers that come from these two registers. The results are stored in the accumulator, the contents of which can be fed to the display device. The keyboard provides the possibility of entering numbers and symbols of operations, that is, commands that must be executed over given numbers.

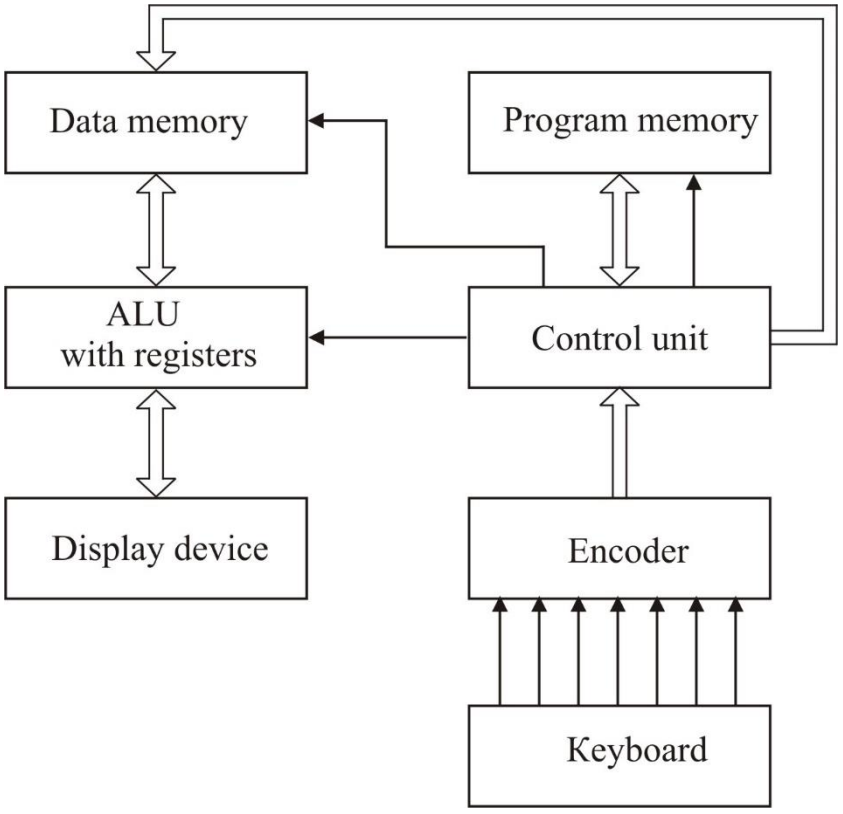


Figure 14.5 – A functional diagram of a programmable calculator

The programmable calculator (Fig. 14.5) contains two memory areas: one for storing data (output and results of intermediate calculations), the other for recording the program, that is, the sequence of control commands or operations that must be performed on the data. The information capacity of the memory can be chosen optimal for this task.

The program is entered from the keyboard through the encoder and control device into the program memory, and the input data into the data memory. In the program execution mode, which is set from the keyboard, the command codes are sequentially selected from the program memory and sent to the control device. On the basis of these codes, the control device produces control signals that, arriving at various devices of the calculator, ensure the execution of the recorded program.

A calculator can be a useful component of a control or computing system. However, its use is limited by the range of performed arithmetic operations.

Microcomputers perform a large set of operations, have a considerable set of peripheral equipment and are therefore widely used in various branches of the national economy.

14.3. Description of the microprocessor laboratory "MICROLAB KP580 IK80"

MICROLAB is a microcomputer with a built-in control panel and is powered by an external 220 V, 50 Hz network. The power supply of the internal units is provided by a built-in source of constant stabilized voltages +5 V, 5 V, 12 V. MICROLAB is a single-board microcomputer, its central processor KP580IK80A is a single-crystal eight-bit parallel microprocessor with a fixed command system and performs the main function of a computer information processing in the system. The microprocessor command system contains 78 basic commands in one-, two-, and three-byte formats. Commands ensure the execution of arithmetic, logical operations, information transfer operations, conditional and unconditional transitions, computer operation control. When forming commands, several types of addressing are used: direct, indirect, stack, implicit.

Input and output of data from the MICROLAB in dialogue mode is carried out using the built-in control panel (keyboard). All information is issued in a sixteen-year code and is displayed on the indicators. These procedures are controlled by the special program MONITOR, which is recorded in the MICROLAB RAM.

The user interacts with the MICROLAB using the keyboard and indicators. Sixteen buttons (O – F) on the right side of the keyboard are used to enter data into the microcomputer in hexadecimal code. When the specified keys are pressed, the corresponding data is displayed on the four right indicators of the display device. The next key that is pressed illuminates the rightmost indicator, and the next digits are moved to the left by one position. The keyboard buttons on the left provide execution of single commands of the Monitor control program. When you press the "RESET" button, you enter the MONITOR. At the same time, zeros are displayed on the indicators of the address register (IAR) and the indicators of the data register (DRI),

scanning is performed – a cyclic survey of the keyboard, which is repeated. Execution of the user program is interrupted.

When pressing the "UST.AD" button, four sixteen-year numbers, which are pre-set in the IRD, are sent to the IAR. At the same time, such a combination of numbers is considered as the address of a memory cell. The contents of the cell with such an address are displayed in the two extreme positions of the IRD, and the digits preceding them are shifted to the left.

When pressing the "AD+" button, the address displayed on the IAR is increased by one, and the data located at this new address is induced by the two rightmost digits of the IRD.

When pressing the "AD-" button, the address displayed on the IAR is reduced by one, and the data corresponding to this new address is also induced by the two rightmost digits of the IRD.

When pressing the "WRITE" button, the two rightmost digits of the IRD (one byte) are entered into the cell whose address was displayed on the four IAR indicators before pressing the "WRITE" button. Immediately after pressing the indicated button, the IAR reading increases by one, and the data previously recorded at this new address is displayed on the two rightmost indicators of the IRD. The data recorded at the previous address is moved to the left by two positions for the convenience of visual recording control.

When the "START" button is pressed, the execution of the user's program starts from the address specified by them on the IAR, and which is actually entered into the microprocessor's command counter. This address must indicate the cell in which the first byte of the first command of the program is stored.

When the "RETURN" button is pressed, the interrupted program, which was started by the "START" command, is executed. At the same time, execution is carried out starting from the address stored in the command counter (regardless of the IAR readings).

The "INPUT" and "OUTPUT" buttons are intended for reading information (programs, data) from an external medium to a computer and, accordingly, for outputting from a computer to an external medium.

The MICROLAB also uses the "STEP - AUTO" mode switch, the two positions of which correspond to automatic (continuous) execution of the user's program and step mode, in which after executing one (each) command of the program, the MICROLAB goes to the MONITOR program, while the execution of the program is interrupted. To continue running the program, press the "RETURN" button.

The stepping mode (tracing) is necessary for debugging programs and is possible due to the availability of the KR580IK80A microprocessor's mode of interrupting its operation. The step mode in MICROLAB is a special case of the calculation mode with interrupting the program at the specified address the specified number of times. Yes, during tracing, an interruption occurs once after the execution

of each command. After each interrupt, the address of the breakpoint is incremented in such a way that it indicates the address of the next command.

The MONITOR program provides the possibility of a dialogue between the user and the controller, serves for entering and organizing program debugging. MONITOR occupies 1024 bytes and is written in the ROM at addresses 0000 – 02FF, 0300 – 03FF, and uses an area in the RAM of 57 bytes at addresses 83C7 – 83FF. The user is allocated a RAM area limited to addresses 8000-8306 for entering written programs, original output data, and calculation results.

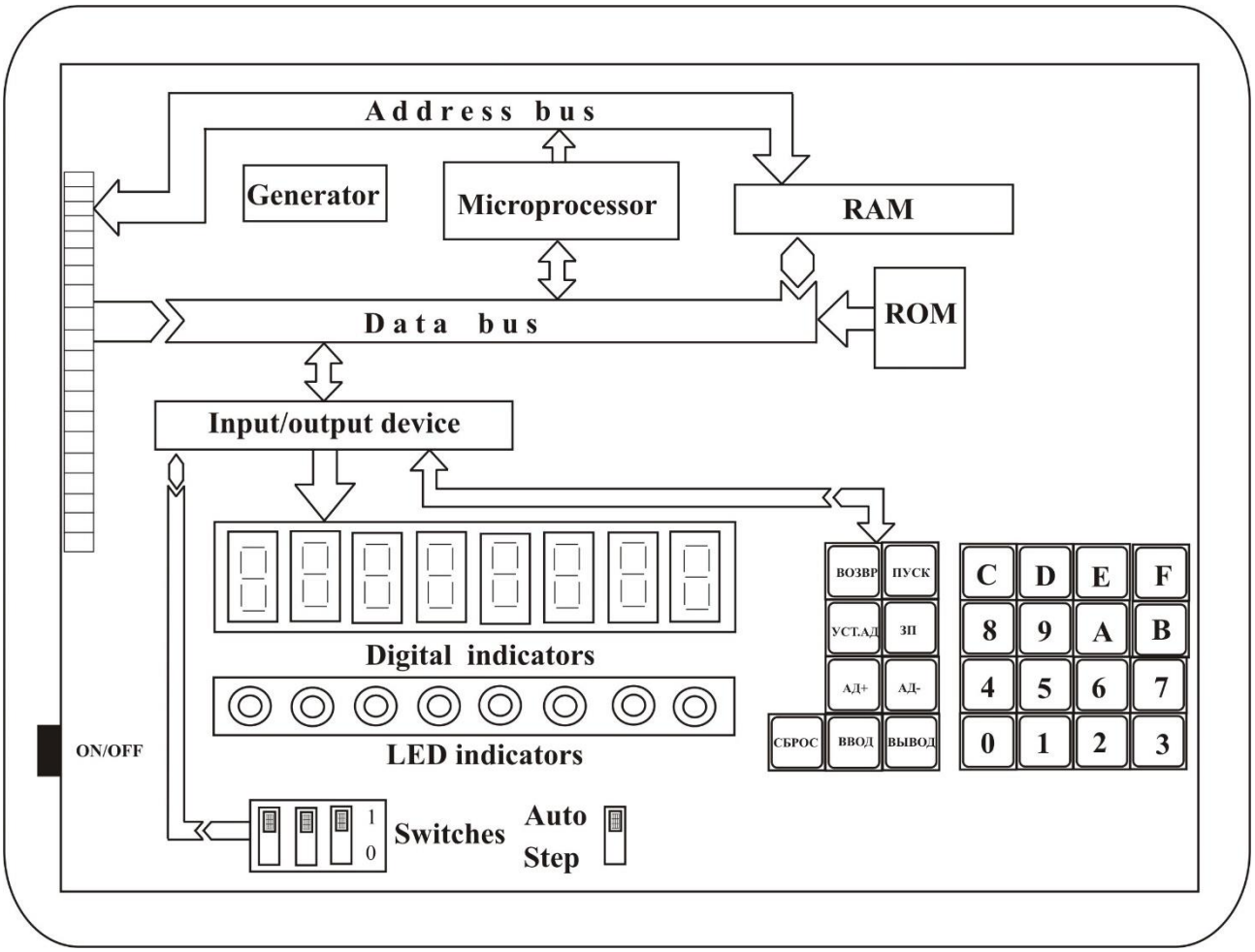


Figure 14.6 – Image of the front panel of MICROLAB

On the front panel, in the upper part, there are microcircuits, devices, and its structural diagram is presented. In the lower part – elements of the control device and input – output of information.

The keys provide control of MICROLAB operation and input of information and have the following purposes:

"СБРОС (RESET)" - resetting the system and returning to the initial position;

"АД (AD+)" - increasing the address by 1 and reading data from memory;

"УСТ. АД. (SET ADDRESS)" - address setting and reading data from memory;

" ВОЗВР. (RETURN)" - return to the implementation of the program, which began at the command of the ПУСК (START);

" ПУСК (START)" - execution of programs from the displayed address;

"ЗП (RECORD)" - writing data to memory and increasing the address by 1;

"AD-" - reducing the address by 1 and reading data from memory;

"ВЫВОД (OUTPUT)" - output of information from memory to an external medium;

"ВВОД (INPUT)" - entering information from an external medium into memory.

0 – F - input of information in hexadecimal code.

The device provides simulation of external sensors and information receivers. As sensors of parallel input, three keys with the position "1 - 0" are provided, which form the level of a logical signal. Receivers of parallel information are eight LED indicators, and a speaker is used as a receiver of serial information (the volume control of the speaker is located on the left in the lower part of the panel).

The device provides the following modes and functions:

• automatic or step mode of program execution, which is selected with the help of the "AUTO-STEP" toggle switch;

• resetting and initializing the system using the RESET key;

• manual output of information to the memory block from the keyboard;

• automatic data output on a digital display in the form of seven-segment digital indicators, eight LED indicators and a speaker;

• control and correction of recorded information;

• execution of the program, starting from any point, and its interruption at any point;

• indication on the panel of the contents of the microprocessor battery and states when the program is stopped during its execution in step mode or in interrupt mode;

• correction of the contents of the accumulator, signs, general-purpose registers of the microprocessor at any step of program execution.

For solving various problems, exchanging information, control, etc. the microprocessor uses a certain "language", which is machine code. MP operates with words, which are a sequence of symbols of a certain length, for example, 8, 16, 32 bits or digits. A bit is a sign of binary information 0 or 1 (electric bit – logic level of signal voltage: 1 – high level, 0 – low level). The length of the words that are processed determines the MP resolution. A group of bits, which can be processed by MP in one work step, creates a machine word or a simple word. The length of a machine word is determined by the number of bits in one memory register. One of the main concepts of "language" is a byte – an eight-bit word used to exchange digital information between MP nodes. In bytes, the length of words and the capacity of a memory block are expressed.

To perform the task, it is necessary to enter and write down the corresponding list of commands to the MP through the keyboard. At the same time, all commands

must be translated into a code that the MP understands and which stores the necessary time in the memory block. MP starts work by reading the first code from the memory block, decodes the corresponding command from the BP and performs the operation indicated there. After that, the MP reads the next command and performs the corresponding operation. This process is repeated with a sequential enumeration of the specified memory cells. Certain commands force the MP to "jump" to another memory address, bypassing the order of priority. The program can return the MP to execute the command from any specified address, forming a loop. This will allow you to create a program with multiple repetition of a number of operations.

4.3.1. Numerical systems. A number system is a set of symbols (numbers) and ways of writing numbers. Depending on the way numbers are written, number systems are divided into non-positional, such as the Roman numeral system, and positional. In the positional numbering system, the value of a digit in a number is determined by its position - the digit of the number. In MP, positional systems are used, in which the value of a digit in a number is determined by its position – the digit of the number. The name of the positional number systems corresponds to the number of digits used in them. In everyday life, we use the decimal numbering system, which uses ten digits from 0 to 9, and MP with the binary system. MICROLAB uses the hexadecimal number system, which more conveniently represents programs and data in binary numbers.

Any positive number A in the decimal system can be written as a series

$$A = a_n \cdot 10^n + a_{n-1} \cdot 10^{n-1} + ... + a_1 \cdot 10^1 + a_0 \cdot 10^0 + a_{-1} \cdot 10^{-1} + ... + a_{-m} \cdot 10^{-m},$$

where 10 – the base of the system системи; $a_n, a_{n-1}, ..., a_{-m}$ – coefficients taking the value 0 to 9; *n* and *m* are any integers.

For example, the number 5108,3 can be represented as

$$5108{,}3 = 5 \cdot 10^3 + 1 \cdot 10^2 + 0 \cdot 10^1 + 8 \cdot 10^0 + 3 \cdot 10^{-1}.$$

In the digital processing of information, the binary numbering system is widely used, in which only two digits are used to record numbers: 0 and 1. Any positive number B in the binary system is written as a series

$$B = b_n \cdot 2^n + b_{n-1} \cdot 2^{n-1} + ... + b_1 \cdot 2^1 + b_0 \cdot 2^0 + b_{-1} \cdot 2^{-1} + ... + b_{-m} \cdot 2^{-m},$$

where 2 – the basis of the system; $b_n, b_{n-1}, \ldots, b_{-m}$ – coefficients taking the value 0 or 1; *n* and *m* are any integers.

The whole part is separated from the small part by a point. For example, the number 3 in the binary system is written in the form

$$3_{10} = 1 \cdot 2^1 + 1 \cdot 2^0 = 11_2$$

The hexadecimal numbering system is used in specialized computers. This system is based on the number 16, so it uses 10 numbers and 6 letters: 0, 1, 2, ..., 8, 9, A, B, C, D, E, F.

To convert a number from the binary to the hexadecimal number system, it is necessary to divide the binary number into groups of four digits (tetrads) to the left and right of the point. Extreme incomplete tetrads are supplemented with zeros, after which each tetrad is replaced by a number of the hexadecimal system in accordance with Table 14.1. Example,

$$11110010_2 = 1111 \quad 0010 = F2_{16}, \text{ since}$$

$$1111_2 = F_{16}, \text{ a } 0010_2 = 2_{16}.$$

To carry out the reverse conversion, it is necessary to replace each symbol of a number from the hexadecimal system with four numbers from the binary system, according to the Table. 14.1.

Table1 14.1 – Decimal, binary and hexadecimal representation of numbers

Decimal system	Binary system	Hexadecimal system	Decimal system	Binary system	Hexadecimal system
1	1	1	18	10010	12
2	10	2	19	10011	13
3	11	3	20	10100	14
4	100	4	21	10101	15
5	101	5	22	10110	16
6	110	6	23	10111	17
7	111	7	24	11000	18
8	1000	8	25	11001	19
9	1001	9	26	11010	1*A*
10	1010	*A*	27	11011	1*B*
11	1011	*B*	28	11100	1*C*
12	1100	*C*	29	11101	1*D*
13	1101	*D*	30	11110	1*E*
14	1110	*E*	31	11111	1*F*
15	1111	*F*	32	100000	20
16	10000	10	33	100001	21
17	10001	11	34	100010	22

For example, the number $C2_{16}$, taking into account that $C_{16} = 11002$, and $2_{16} = 00102$ takes the form

$$C2_{16} = 1100\ 0010 = 11000010_2.$$

The binary system is widely used in digital technology due to the fact that an element with two stable states 0 and 1, for example, an electronic key, is needed to represent one digit of a number.

Arithmetic operations with two numbers are performed in accordance with the rules given in Table 14.2.

Table 14.2 – Rules for the calculation of arithmetic operations with binary numbers

Binary addition	Binary subtraction	Binary multiplication
0 + 0 = 0	0 - 0 = 0	0·0 = 0
0 + 1= 0	1 - 0=1	0·1=0
1 + 0 = 1	1 - 1 = 0	1·0 = 0
1 + 1 = 10	10 - 1 = 1	1·1 = 1

14.3.2. Organization of MP system memory. In the MP system, the memory is designed to store information and is divided into main (internal) and additional (external). Main memory is organized by bytes or words into a group of cells, each of which has its own address. Non-storage devices (SD) of internal memory are divided into two categories: non-volatile storage devices read-only memory (ROM) and random access memory (RAM). RAM is a memory in which data can be stored and changed. ROM is a memory from which information can be read. In order to process data in a certain order, stacks are used. Stacks are storage devices in which a data element can only be added to or removed from its upper cell.

The MP RAM of the MICROLAB laboratory is built on the K565RU2 microcircuit using a RAM with a capacity of 1024 bits (128 bytes). To obtain an 8-bit word, eight such SD are required. The MICROLAB ROM is implemented on two KR556RT5 bi-polar microcircuits with 512x8 bit organization. In the Table 14.3 shows the memory card of the MP laboratory for each device. The user RAM reserves addresses from 8000 to 83FF, that is, 8000 is the address of the first free memory cell, and 83FF is the address of the last available cell.

Table 14.3 – Memory card in the MICROLAB KP580 IK80

Address in hexadecimal sustem	Capacity of memory, bytes	ROM or RAM	Using
0000 – 05FF	1024	ROM	Control program area (MONITOR area)
0600 – 7FFF	31232	–	An area that is not used
8000 – 8306	967	RAM	User area

Continuation of Table 14.3			
Address in hexadecimal sustem	Capacity of memory, bytes	ROM or RAM	Using
8307 – 83FF	57	RAM	MONITOR working area
8400 - FFFF	31744	–	An area that is not used

Commands and data in the MP system are presented in the same form, that is, in the form of binary numbers, which are stored in memory and transmitted over the data bus in the MP. This way of writing programs is called machine language programming. If instead of binary codes to represent commands, registers, memory cells, data, some of their symbolic names are used, then we will get a program in the Assembler language. Symbolic names are usually mnemonic. This means causing associations with functions performed by commands, or with the assignment of registers or memory cells.

The machine language is usually determined by the MP assignment and cannot be changed. The Assembler is created during the production of the MP for the convenience of the programmer, but is not expected by the purpose of the device. In order to avoid the dependence of programs on the architecture and command system of specific MP systems and to facilitate programming, procedurally oriented languages or high-level languages were created. These languages have such capabilities that the problems to be solved can be presented quite easily in a form that is understandable to a special translator program that translates the program from a high-level language to machine language. The most common high-level languages include FORTRAN, BASIC, PASCAL, C, and others.

Only machine language programs are directly entered into MICROLAB. For machine codes, hexadecimal representation is used because it is easier compared to binary. MICROLAB has internal mathematical support for automatic translation from hexadecimal to binary code. Reading from the keyboard, performing the selected operation, controlling the display is carried out under the control of the Monitor program.

14.3.3. Methods of working with the MICROLAB device. Before starting work, it is necessary to carefully familiarize yourself with the location and purpose of the controls and indicators on the front panel of the device (see Fig. 14.6). The MICROLAB is located in a portable housing. The general power supply of the device is carried out from a single-phase voltage network of 220 V, 50 Hz. Connection to the network is carried out through a connecting cord with a standard two-pole plug. The "NETWORK" switch must be in the on position before connecting to the network.

***To start working with the device, you need*:**

- connect the power cord to the network;
- set the "AUTO/STEP" switch to the "AUTO" position;
- set the "NETWORK" switch to the "ON" position;

- wait 2-4 minutes for the device to enter operating mode;

- press the "RESET" button and zeros should be displayed on all eight indicators of the digital board;

- after that, you can start checking the device's performance.

As a test task, we use the program recorded in the ROM. This program is stored in the memory of the MICROLAB, starting at the memory cell with the address 0300.

To start the program, you need:

1) press buttons 3, 0, 0, i.e. number 300;

2) press the "SET AD" button the number 300 is displayed on the left indicators, and the two rightmost indicators display what is stored in the cell with the address 0300.

3) press the "START" button of the program execution, which is written in the memory from address 0300, begins.

4) it is possible to stop the execution of the program by pressing the "RESET" button.

Memory check, data recording and storage:

press the "RESET" button;

1) press buttons 8, 0, 0, 0 and "UST.AD". The four left digits of the display show the address just entered, and the last two right digits show the data stored at that address. The address and data displayed on the display are expressed in hexadecimal code;

2) press the "AD+" button. The left indicators will increase the address, and the two rightmost indicators will show the contents of the next memory cell. By repeatedly pressing the "AD+" button, you can view the contents of the memory;

3) press the "AD-" button. The address is decremented by 1 on the left indicators, and the contents of the memory cell corresponding to this address are displayed on the two rightmost indicators. Thus, by pressing the "AD-" button, you can view the contents of the memory in reverse order.

Starting and interrupting programs, step-by-step and automatic execution of them

When the "START" button is pressed, the execution of the program starts from the address displayed on the indicators. This address must point to the memory cell that holds the first byte of the command, but not the data or jump address. MICROLAB can execute both user programs and standard programs. The device has two operating modes: automatic and step mode. The step operation mode is important when observing the state of the system after it executes each command of the user program in the process of checking and debugging this program. The "STEP/AUTO" switch is used to select one of these operating modes.

When switching the work mode toggle switch to the "STEP" position, after executing each command (for its execution, you need to press the "START" button), the execution of this program is interrupted in the user program. At the same time, the display shows the address of the next command and the contents of the memory cell

with this address. The contents of the memory cells with the addresses of jumps and data that were used during the execution of the command do not appear on the display.

When switching the work mode switch to the "AUTO" position and pressing the "START" button, the program starts running in automatic mode. At the same time, only those data whose output is provided by the user can appear on the display. The "RESET" button stops program execution at any position of the operating mode switch, zeros appear on the display and MICROLAB is ready to enter new data.

14.3.4. Programming the output of signals to LEDs. The task of lighting a combination of LEDs. Output indicators (LEDs) VD1….VD8 are connected to the data bus using a programmable peripheral interface. Examples of certain combinations of lighting LEDs and binary and hexadecimal codes corresponding to these combinations are given in the Table 14.4. A one in the binary code of the signal means the LED is lit.

Table 14.4 – LED lighting order

Binary code								Hexa-decimal code
VD1	VD2	VD3	VD4	VD5	VD6	VD7	VD8	
1	0	0	1	0	0	1	0	92
0	1	0	0	1	0	0	1	49
0	0	1	0	0	1	0	0	24

To program the interface, the MVI A, 81 command loads code 81 into the accumulator, and after that, the OUT FB command writes the contents of the accumulator to the FB address. The selected hexadecimal code for lighting the LEDs (for example, 92) is written by the MVI A, 92 command to the battery. The OUT F9 command outputs the battery data at address F9. Stopping the program is carried out by the HLT command. An example of a program that implements the given algorithm for lighting a given combination of LEDs is given in Table. 14.5.

Table 14.5 – LED lighting order program

Address	Code	Command	Commentary
8000	3E	MVI A, 81	Programing of the interface
8001	81		
8002	D3	OUT FB	
8003	FB		
8004	3E	MVI A,92	To set 1,4,7 LEDs lighting
8005	92		
8006	D3	OUT F9	
8007	F9		
8008	76	HLT	Stop

The operation of the main "running lights" program must be ensured by a delay routine that determines the ignition time of each LED combination. First, the delay value (number N) is set in the accumulator and the LOOP delay routine is called (by the CALL LOOP command). The accumulator is decremented (by the DCR A command) until it reaches zero, after which control is returned to the calling program (the RET command). The end of account condition is checked by the JNZ command. The delay time is defined as follows 0,5 [14(N-1) +21] μs. The largest delay is caused by setting the accumulator to zero, which is equivalent to N = 256. Thus, the maximum delay is 1795 μs.

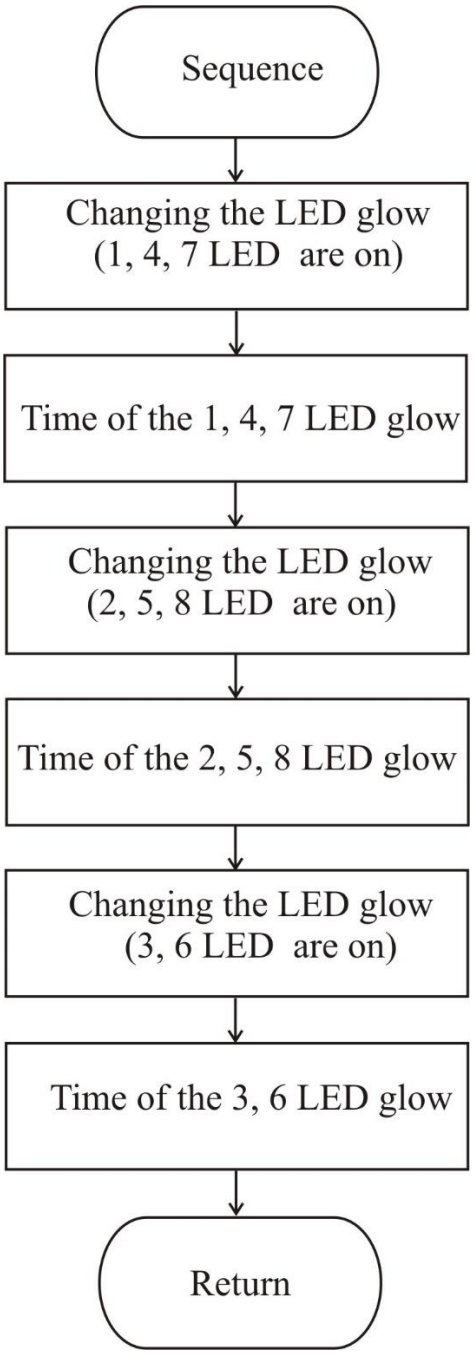


Figure 14.7 – Algorithm of the program «running lights»

To increase the time delay, two delay loops (outer and inner) are organized in such a way that the outer loop determines how many times the delay is executed by the inner loop. The LEDs of the output port are used as "running lights" simulators.

The controller regulates a certain sequence of alternating lighting of selected combinations of light-emitting diodes. The algorithm of the controller is shown in Fig. 14.7.

An example of the "running lights" program, which implements the algorithm in Fig. 14.7, given in the Table 14.6. The time delay routine consists of two loops as described earlier, with the inner loop generating a delay of 0,786 sec and the outer loop executing once.

Table 14.6 – "Running lights" program

Address	Code	Label	Command	Commentary
8000	3E		MVI A,81	Programing of the interface
8001	81			
8002	D3		OUT FB	
8003	FB			
8004	3E	SEQ	MVI A, 92	To set 1,4,7 LEDs lighting
8005	92			
8006	D3		OUT F9	
8007	F9			
8008	16		MVI D, 1	Lightning the sequence
8009	01			
800A	CD		CALL DELAY	
800B	22			
800C	80			
800D	3E		MVI A, 49	To set 2,5,8 LEDs lighting
800E	49			
800F	D3		OUT F9	
8010	F9			
8011	16		MVI D, 1	Lightning the sequence
8012	01			
8013	CD		CALL DELAY	
8014	22			
8015	80			
8016	3E		MVI A, 24	To set 3,6 LEDs lighting
8017	24			
8018	D3		OUT F9	
8019	F9			
801A	16		MVI D,1	Lightning the sequence
801B	01			
801C	CD		CALL DELAY	
801D	22			
801E	80			
801F	C3		JMP SEQ	Return to the main program
8020	04			
8021	80			
8022	01	DELAY	LXI B,00,00	The start of internal loop of delay

Continuation of Table 14.6

Address	Code	Label	Command	Commentary
8023	00			
8024	00			
8025	0B	LOOP	DCX B	Internal loop which generates delay of 0,786 sec
8026	78		MOV A, B	
8027	B1		ORA C	
8028	C2		JNZ LOOP	
8029	25			
802A	80			
802B	15		DCR D	External loop of delay
802C	C2		JNZ DELAY	
802D	22			
802E	80			
802F	C9		RET	Return

14.4. Formulation of the problem

14.4.1. Conduct an experiment on lighting a certain combination of LEDs, performing the following actions:

- enter the program from Table 14.5 into the MICROLAB memory;
- make sure that the program is correctly recorded in the memory;
- execute the program starting from address 8000;
- after making sure that LEDs 1, 4, 7 are lit, stop the program execution by pressing the "RESET" button (otherwise, it is necessary to find and correct errors in the program).

14.4.2. To ensure the burning of another combination of LEDs, change the program, make appropriate changes in the MICROLAB memory, and then execute the changed program.

14.4.3. Conduct an experiment on the implementation of the "running lights" program by performing the following actions:

- enter the program from Table 14.6 into the MICROLAB memory.;
- make sure that the program is correctly recorded in the memory;
- execute the program starting from address 8000;
- visually verify the operation of the program by "running lights" (otherwise, it is necessary to find and correct errors in the program);
- will stop the execution of the program by pressing the "RESET" button.

Control Questions

1. What are microprocessors? Draw a structural diagram and explain the operation of a microprocessor system.

2. What are single-chip and multi-chip microprocessors?

3. What is a bit, digit, machine word, byte?

4. Draw a structural diagram and explain the operation of a microprocessor.

5. Name the three main components of a microprocessor. How is communication between them carried out?

6. What is an arithmetic logic device and why is it needed? Here are its main operations.

7. Name the main buses in a microprocessor and explain their purpose.

8. Name the main registers in a microprocessor and explain their purpose.

9. What is a command counter? Explain its work.

10. What is a register or a flags register? Explain its work.

11. What is a status register? Explain its work.

12. What are general-purpose registers? Explain their work.

13. What are stack registers? Explain their work.

14. What is a clock pulse generator? Explain its purpose.

15. Name the microprocessor command system and explain their purpose.

16. Draw and explain the generalized structural diagram of a microprocessor command.

17. Name the main commands of arithmetic and logical operations.

18. Name the purpose and explain the work of forwarding commands.

19. Name the purpose and explain the work of control commands.

20. What is a microcomputer? Name their main types.

21. Draw a block diagram of a simple calculator and explain its operation.

22. Draw a block diagram of a programmable calculator and explain its operation.

Laboratory work 15

STUDY OF LOGICAL ELEMENTS, LOGIC OPERATIONS AND TRIGGERS

15.1. Purpose of the work

The purpose of the work is the study of basic logical elements, the study of correspondence tables of logic operations and their implementation with the help of logical elements. And also, the purpose of the work is to study the principle of operation, basic parameters and characteristics of trigger circuits, study of compatibility tables of various types of triggers.

15.2. Description of universal laboratory bench LOGIC and TRIGGER

The LOGIC training and laboratory bench is a software and hardware complex that allows students to consolidate their theoretical knowledge in practice, and either gives a more complete idea of the principle of operation of logical elements and combinational circuits based on these logical elements. The bench is powered by 220 V alternating voltage network through the power supply unit.

The bench, the appearance of which is shown in Fig. 15.1, includes:

– a set of logical elements implemented on microcircuits of the 74NS series;

– dynamic indication in the form of two seven-segment indicators;

– two built-in voltmeters;

– a generator of single pulses (single vibrator), which is controlled by the "Select" button;

– four triggers controlled by the “Fix” buttons;

– generator of rectangular pulses, which is controlled by variable resistor "Generator";

– a direct voltage source of 0….5 V, which is controlled by the “Voltage In” variable resistor;

– four-digit pulse counter;

– connector for turning on the oscilloscope;

– logical level indicators in the form of LEDs.

The appearance of the TRIGGER bench is shown in Fig. 15.2. The bench includes:

– a set of elements is implemented on microcircuits of the 74NS series;

– dynamic indication in the form of 2 four-digit seven-segment indicators;

– generator of single pulses (single vibrator), which is controlled by the Impulse/Generator button;

– four triggers controlled by the “Fix” button;

– generator of rectangular pulses, which is controlled by buttons F+, F-;

– four-digit pulse counter;

– 2 connectors for connecting to the oscilloscope;

– logical level indicators in the form of LEDs.

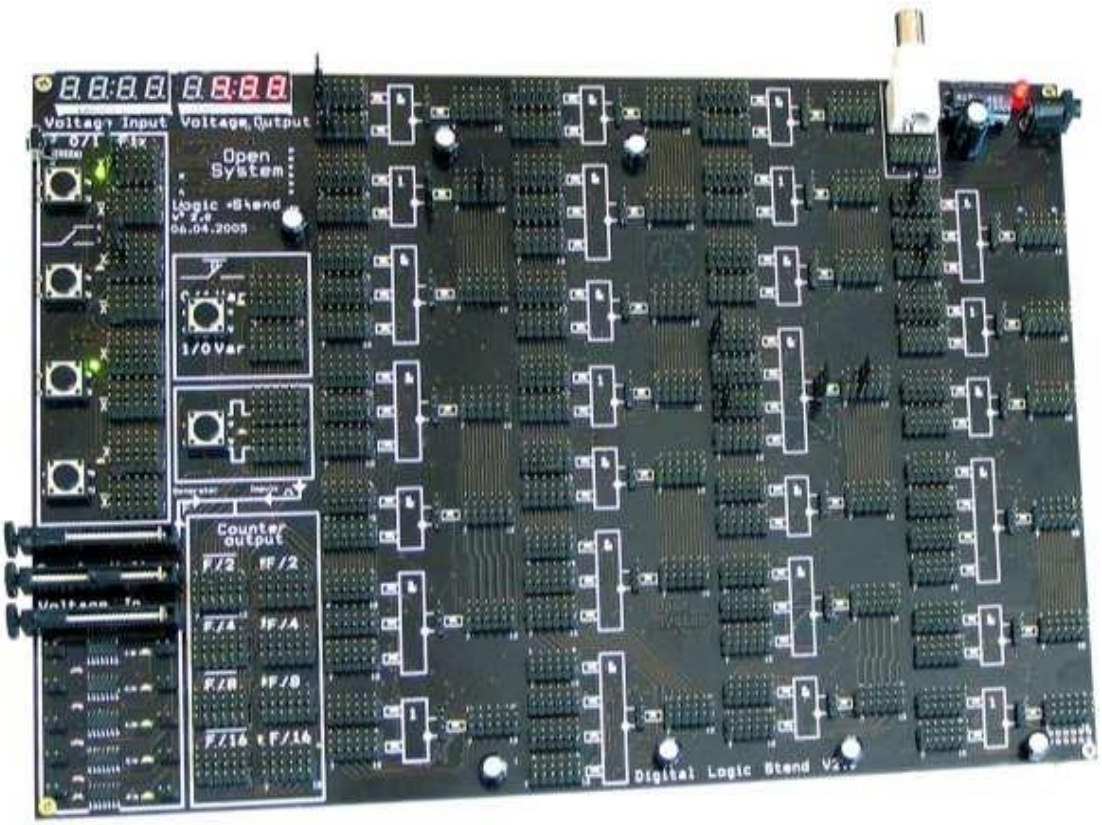


Figure 15.1 – Appearance of the LOGIC laboratory bench

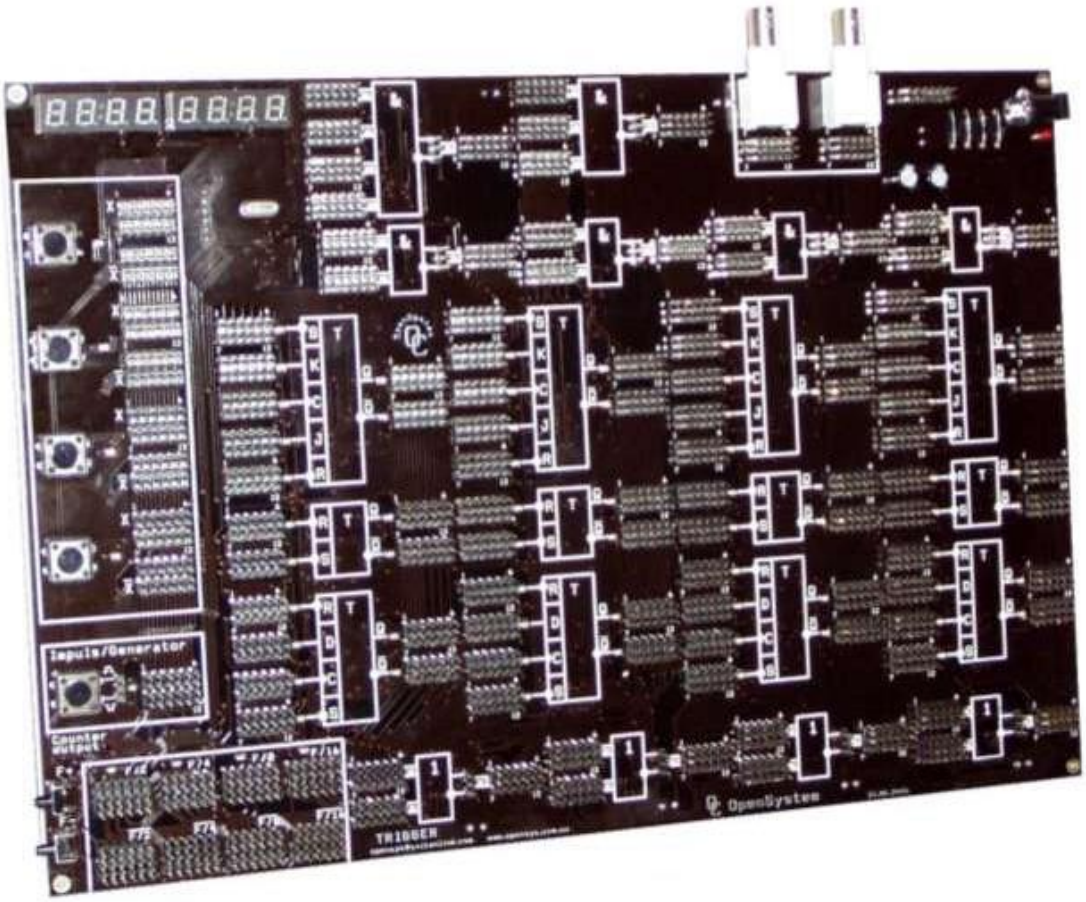


Figure 15.2 – Appearance of the TRIGGER laboratory bench

As can be seen from Fig. 15.1 and Fig. 15.2, all functional circuits intended for research are located in the central area of the device and occupy most of it. For a better visual perception of each functional circuit, its schematic diagram is presented on the front panel. In the places where the input and output images of the circuit are displayed, corresponding LEDs are installed that show the signal level (lighting LED – high level, non-lighting LED – low level).

The power supply unit is located in the upper right part of the laboratory benches. Nearby is a connector for connecting external control and measuring equipment. The internal power supply unit of the laboratory model provides +5V supply voltage. Voltmeters measure voltages in the range from 0 V to 6 V, with an error of 0,02 V. Variable resistors allow you to vary the voltage from 0 V to +6 V.

With the help of switching fields located on the benches, combinational circuits are synthesized. With the help of control elements at the inputs of logic elements and combinational circuits, the required sequence of logic levels is set. The structural diagram of the block of logical elements and control elements is presented in Fig. 15.3.

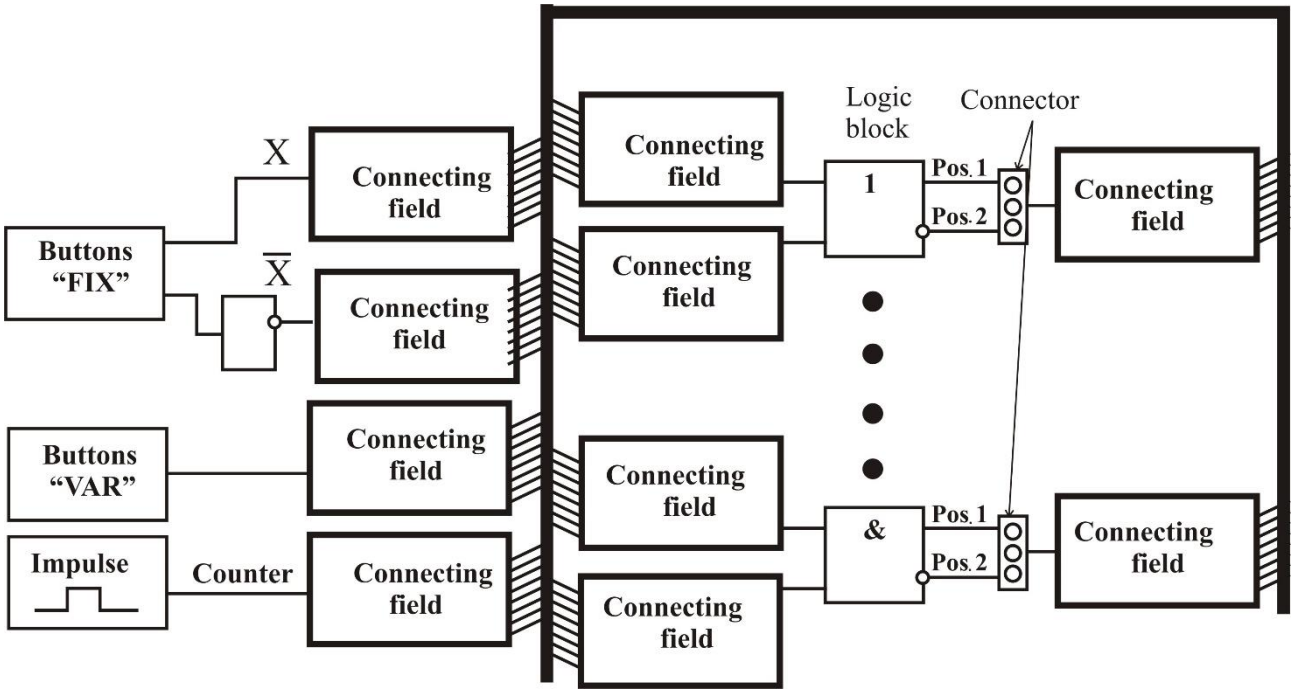


Figure 15.3 – Structural diagram of a block of logical elements and control elements

The "FIX" buttons change their state (logical level) to the opposite each time the button is pressed according to the trigger principle, i.e. pressing the button means that a high level signal is applied to the switching field – logical one, and releasing the button means that a low level signal is applied – logical zero . The "VAR" buttons do not store the logic level. A logical unit appears on the switching field when this button is pressed and vice versa. The "Impulse" button controls the single-vibrator, which forms a pulse of approximately 20 ms.

The pulse can be applied to the input of each logical element or to the counter-distributor ("Counter Output"). Next to each “FIX” button there are two switching fields: field X (input signal is not inverted) and field $\overline{X}$ (the input signal is inverted).

The output of the logical elements (see Fig. 15.3) is a connector with three pins, and: pos. 1 – the signal is not inverted, pos. 2 – the signal is inverted.

The connection of logic control elements with the inputs of logical elements and logical elements among themselves in combination circuits is carried out using 12 independent lines on the switching field. The necessary line is selected by placing a jumper on the switching field (see Fig. 15.4).

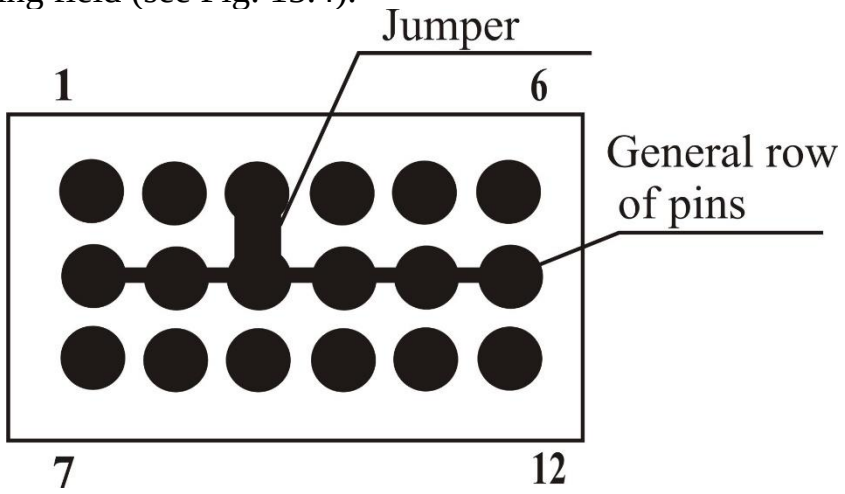


Figure 15.4 – Switching field

12 internal communication lines were used to organize internal communications between individual blocks of the laboratory bench. The constructive implementation of the connection between the elements on the bench is carried out with the help of a switching field. Figure 5 shows an example of a switching field located near a logic element. This is a set of 18 pins (contacts), namely 3 rows of 6 pins. The middle horizontal row is called common. This row of contacts is interconnected by the input or output of the corresponding block of the bench. Two pins connected by a jumper are called a line. One of these pins must be on a common row. The lines are numbered from the first to the sixth and from the seventh to the twelfth line, next to which the corresponding digital marks are placed on the bench. To connect the input or output to the corresponding line, you need to put a jumper on one of the central pins and pins with the corresponding number on the outer lines. Any line can be used for signal transmission. For example, let's choose line No. 3, which is shown in Fig. 15.4.

The bench also has switching fields with 6 pins in four rows, which are located near the “FIX”, “VAR”, “Impulse”, “Counter Output” control buttons. In this case, the line should be selected so that the jumper connects one of the outer and one of the inner rows.

With the help of jumpers, any of the lines can be connected to the input or output of any functional circuit, internal control and measuring device. The contacts are placed in the extreme rows and each is connected to its own communication line.

15.3. General theoretical provisions of pulse devices, logical elements and logic operations, triggers

15.3.1. Pulse mode. Continuous operation requires a long exposure to the signals. The pulse mode of operation is characterized by a short-term influence of the signal, alternating with a pause.

The advantages of pulsed mode in relation to long-term:

1) high power during the pulse with a small average power of the device;

2) the influence of temperature and dispersion of parameters of semiconductor devices is weakened (modes: “on”, “off”);

3) increases the bandwidth and noise immunity of electronic equipment.

Bandwidth is the highest possible speed of information transfer.

Immunity is the ability of the equipment to distinguish signals with a given reliability.

4) to create pulsed devices requires a greater number of simple elements of the same type, easily performed by the methods of integrated technology. This increases reliability, reduces the weight and dimensions of the device.

Pulse devices are used in microprocessor technology, automatic technology, radar, industrial electronics, etc. Pulses (video pulses) of various shapes are used as shown in Fig. 15.1.

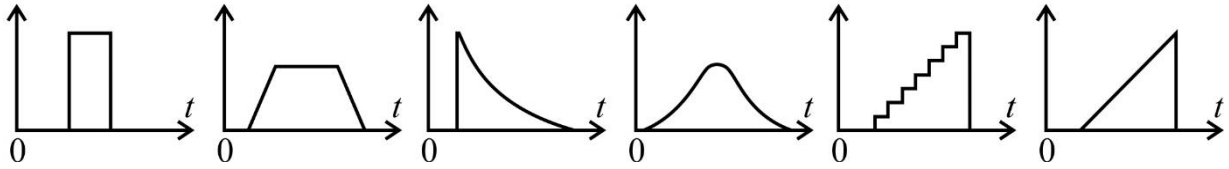


Figure 15.1 – Video pulses

Radio pulses are packets of high-frequency modulated oscillations (Fig. 15.2).

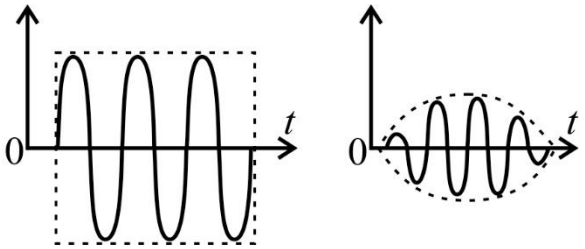


Figure 15.2 – Radio pulses

Pulse technology typically uses video pulses. Pulses usually follow periodically as shown in Fig. 15.3.

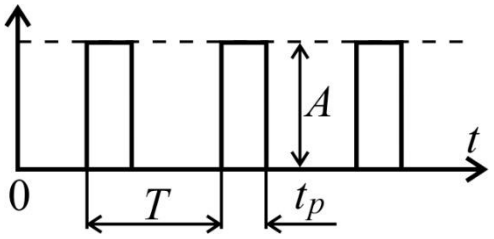


Figure 15.3 – Pulse duty factor

T is the pulse repetition period; t_p is pulse duration or the pulse width (pulse active time). The coefficient q is

$$\boxed{q = \frac{T}{t_p}}$$

This ratio is frequently considered, but the reciprocal value is also used. It is called is pulse duty factor $D = t_p / T$.
(*Electropedia*: *the ratio of the average pulse duration to the reciprocal of the pulse repetition frequency in a pulse sequence*)

In automation, the coefficient q is q = 2...10, and in radar, q is up to 10^4 and higher.

15.3.2. Electronic keys and simple shapers pulse signals. Many pulsed devices include electronic keys. The basis of the electronic key is the active element (semiconductor diode, transistor, electronic lamp) operation in the key mode. The key mode is characterized by two key states: “On” but “Off”. The simplest type of electronic key is a diode key.

Circuit of a serial diode switch with a zero level of inclusion and its transfer characteristic are shown in Fig. 15.4.

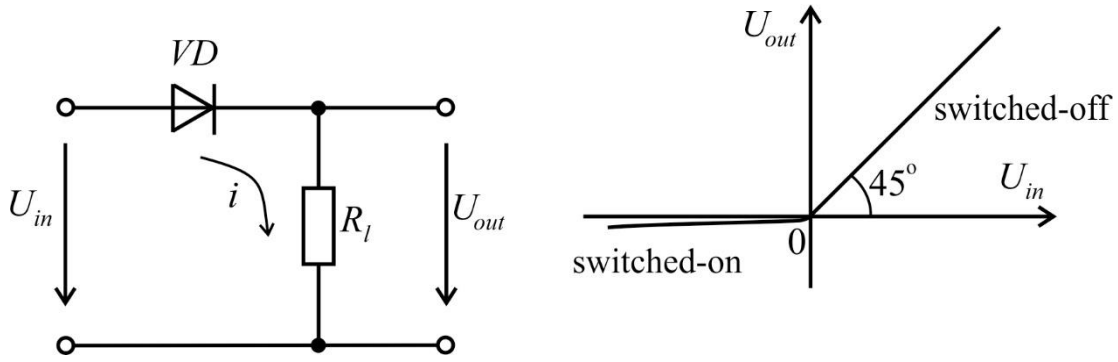


Figure 15.4 – Circuit of a serial diode switch and its transfer characteristic

With a positive input voltage, the diode is open and the current is:

$$i = \frac{u_{in}}{R_{fr} + R_l}, \qquad u_{out} = R_l \cdot i = R_l \frac{u_{in}}{R_{fr} + R_l},$$

where R_{fr} is diode resistance in the forward direction;

R_l is the resistance of the load.

Usually, $R_{fr} << R_l$ then $u_{out} \approx u_{in}$.

With a negative input voltage:

$$i = \frac{u_{in}}{R_{back} + R_l}, \qquad u_{out} = R_l \cdot i = R_l \frac{u_{in}}{R_{back} + R_l}\ .$$

Since $R_{back} >> R_l$, then $u_{out} \approx \frac{R_l}{R_{back}} u_{in} << u_{in}$,

where R_{back} is the resistance of the diode in the opposite direction.

When the polarity of the diode changes, the function graph $u_{out}(u_{in})$ will rotate by 180°.

To change the level of inclusion in the key circuit, a bias source E_0 is introduced (Fig. 15.5).

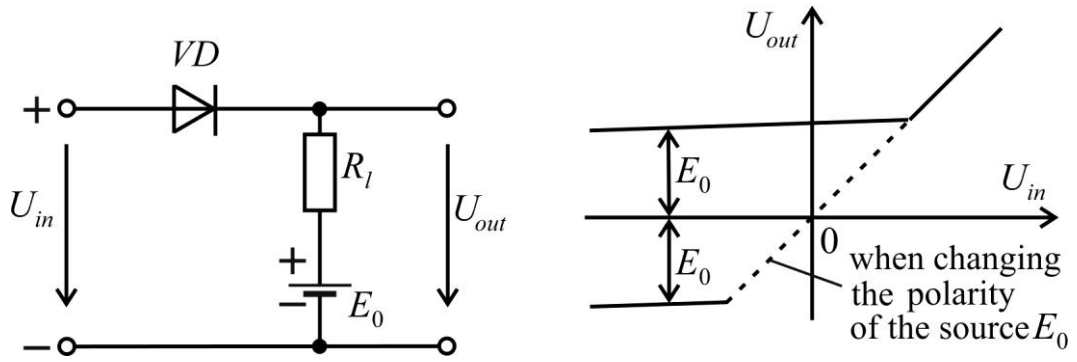


Figure 15.5

When $u_{in} > E_0 \Rightarrow u_{out} \approx u_{in}$ the diode *VD* is open.

When $u_{in} < E_0 \Rightarrow u_{out} \approx E_0$ the diode *VD* is closed.

15.3.3. Circuit of a parallel diode key (Fig. 15.6). With a positive input voltage, the *VD* diode is open (the key is closed) and; at negative voltage the *VD* diode is closed (the key is open). When you turn on the source E_0 (the key with a non-zero level of switching), the level of the closed voltage increases.

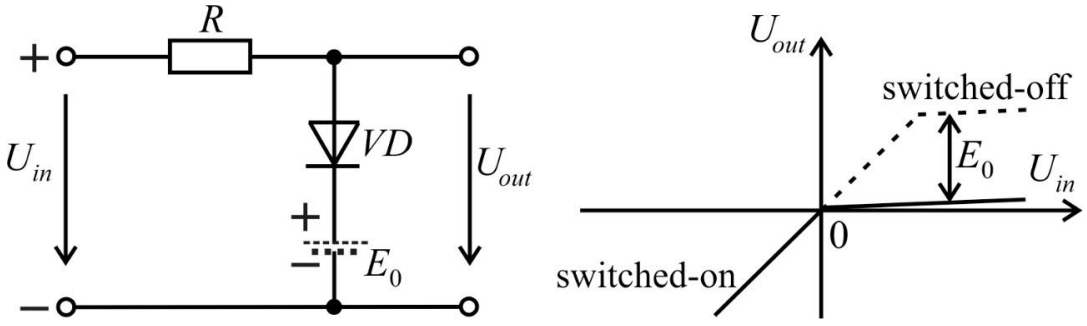


Figure 15.6 – Parallel diode key

15.3.4. Dual diode key circuit (Fig. 15.7)

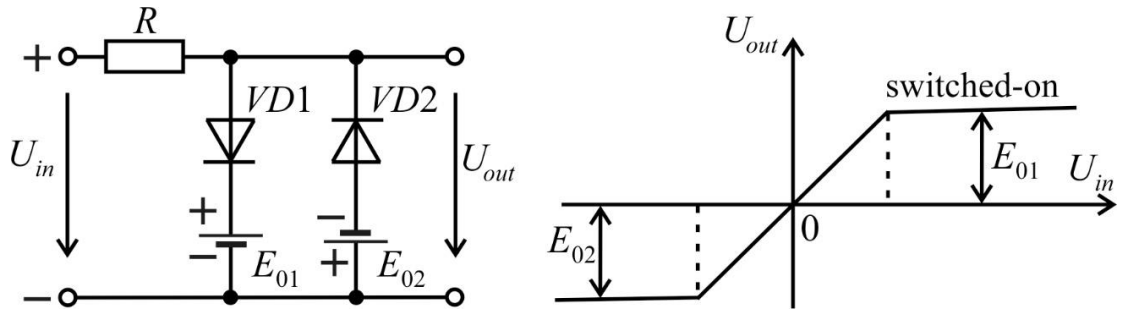


Figure 15.7 – Dual diode key

15.3.5. Transistor switch. Diode keys do not allow to separate the control and controlled circuits, which is often required in practice. In these cases, transistor switches are used.

The key circuit with a bipolar junction junction transistor and characteristics of the operation mode is shown in Fig. 15.8.

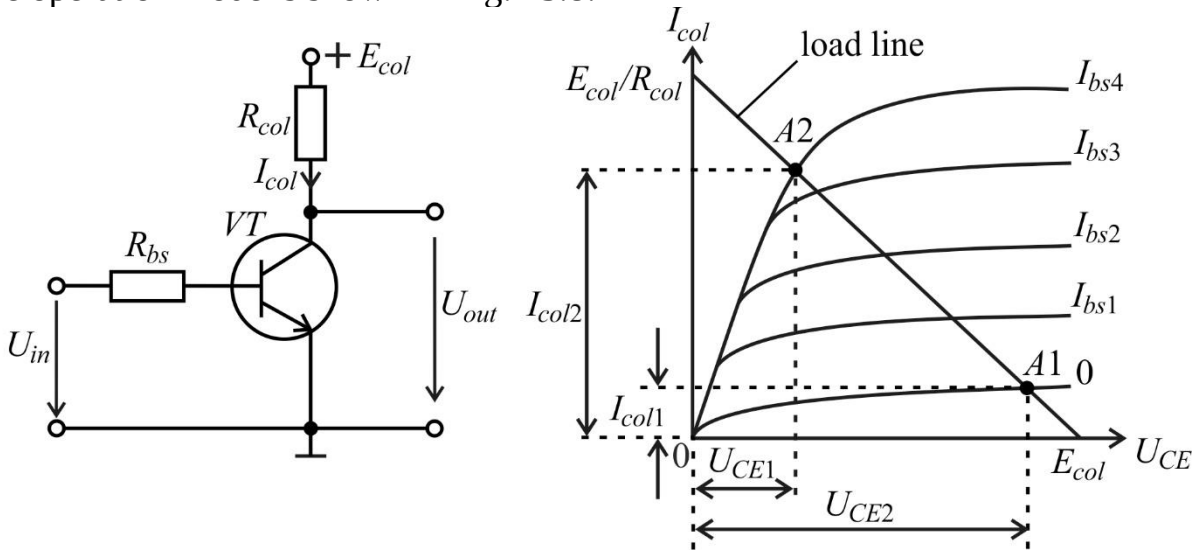


Figure 15.8

The input (control) circuit is separated from the output (controlled) circuit. The transistor operates in a key mode, characterized by two states:

1) The first state is determined by point A_1 on the output characteristics of the transistor. It is called a cut-off mode.

In this case, the base current is $I_b = 0$. The collector current I_{col1} is equal to the initial current I_{col0}, but $U_{col} = U_{col1} \approx E_{col}$. The mode is realized at negative base potentials.

2) The second state is determined by point A_2 on the output characteristics of the transistor. It is called the saturation mode. It is realized with the positive potentials of the base.

The base current is determined mainly by the resistor R_b:

$$I_{b2} = \frac{U_{in}}{R_b} \ ,$$

because the resistance of the open emitter junction is small. Collector junction is also open $I_{col2} \approx \frac{E_{col}}{R_{col}}$ and collector voltage $U_{col2} \approx 0$.

From the cutoff mode to the saturation mode, the transistor is transferred by the action of a positive input voltage. An increase in the input voltage (base potential) corresponds to a decrease in the output voltage (collector potential) and vice versa. Such a key is called an inverting (inverter).

15.3.6. Logical elements and logic operations. Logical elements form the basis of digital (discrete) information processing devices – computers, etc.

A logic operation (function) converts, according to certain rules, input information into output according to the rules of mathematical logic, i.e. Boolean algebra or Boolean logic.

Logical elements are built on the basis of electronic devices operation in a key mode. Digital information is used in binary form: "0" (logic zero) and "1" (logic unit), corresponding to two key positions. Thus, a logic function is a function of logical variables that can take two values: "0" (logical zero) and "1" (logical one). Logic elements are devices that implement one or another logic function. Logic transformations of binary signals contain three elementary operations: OR, AND, NOT.

Logical transformations of binary signals include three elementary operations:

1) OR – logical addition (disjunction), denoted by the signs "V" or "+":

$$F = x_1 \text{ V } x_2 \text{ V } x_3 \text{ V } \ldots \text{ V } x_n$$

2) AND – logical multiplication (conjunction), denoted by the signs "Λ" or "·":

$$F = x_1 \Lambda\, x_2 \Lambda\, x_3 \Lambda\, \ldots \Lambda\, x_n..$$

3) NOT – logical negation (inversion), denoted by a bar over a variable:

$$F = \bar{x}.$$

The logical NOT operation cancels the input signal, transforming it into its opposite at the output. A true statement turns into a false one or vice versa, for example, "1" into "0", or "0" into "1".

In addition to the simplest logic operations, more complex ones can be used. The most important of them are:

4) NOR (NOT-OR) is the negation of logical OR (non-disjunction). It is the negation of a disjunction (Pierce's operation), which is denoted as follows

$$F = \overline{x_1 \text{ V } x_2 \text{ V } x_3 \text{ V} \ldots \text{V } x_n}\,.$$

The NOR operation creates a complex statement from simple ones according to the rule: a complex statement is true only if all the simple statements that form it are false, and false if at least one of the simple statements is true.

5) NAND (NOT-AND) is the negation of a conjunction (Sheffer stroke), which is denoted as follows

$$F = \overline{x_1 \Lambda x_2 \Lambda x_3 \Lambda ... \Lambda x_n}.$$

The NAND operation creates a complex statement from simple ones according to the rule: a complex statement is true if at least one of the simple statements is false, and false if all simple statements are true.

6) INBHIT, which is symbolically written in the form

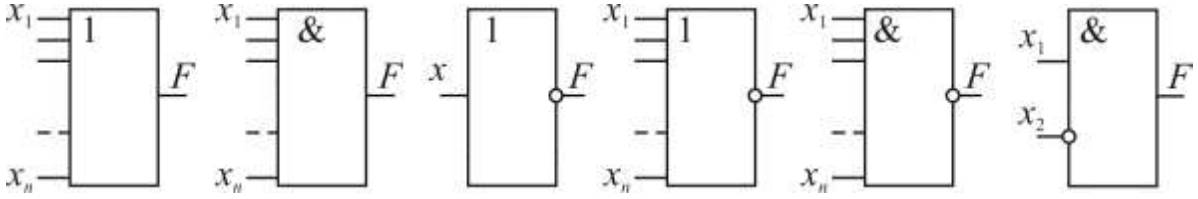
$$F = x_1 \Lambda \overline{x_2}.$$

The INHIBIT operation is a complex statement that is true only when the first of the two statements is true and the second is false. The rules for performing logical operations on binary variables for the case of two variables are presented in Table 15.1.

Table 15.1 – Results of the basic logic operations

x_1	x_2	F					
		OR	AND	NOT (from x_1)	NOR	NAND	INHIBIT
0	0	0	0	1	1	1	0
0	1	1	0		0	1	0
1	0	1	0	0	0	1	1
1	1	1	1		0	0	0

The implementation of the considered logical operations is done with the help of logical elements, the conventional designation of which is given in Fig. 15.9.



a *b* *c* *d* *e* *f*

Figure 15.9 – Conventional designations of the main logical elements implementing logic operations: *a* – OR; *b* – I; *c* – NOT; *d* – NOR; *e* – NAND; *f* – INHIBIT

Where sign ° means that the input (output) is inverse. Depending on the type of signals used, the logic elements are divided into potential and pulse. In potential elements, logical “0” and “1” are represented by two different levels of electric potential, and in impulse ones, by the presence or absence of impulses (the most common are potential ones). Potential logical elements became the most widespread.

In addition, there are such logic operations as XOR (EXCLUSIVE OR) and XNOR (EXCLUSIVE NOR), their implementation on logical elements is shown in Fig. 15.10.

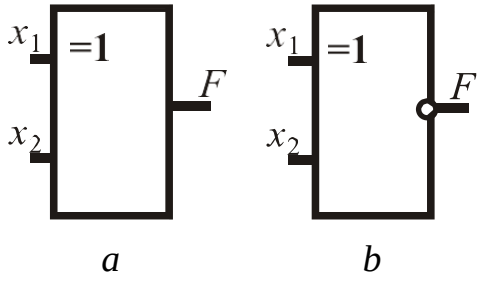


Figure 15.10 – Logical elements implementing logic operations:
a – XOR; *b* – XNOR

XOR is a logic operation (inequality, inversion of equality) provides a unit at the output only when an odd number of units is present at the input of the logical element. Zero at the output when there is an even number of units at the input. The logic XOR operation is written as

$$F = \overline{x_1} \Lambda x_2 \mathrm{V} x_1 \Lambda \overline{x_2}\,.$$

For the function XNOR (EXCLUSIVE NOR) (equivalence) on the contrary – the output is one when the input of the logic element has an even number of units. Zero at the output only when there is an odd number of units at the input. The logical operation XNOR is written as

$$F = x_1 \Lambda x_2 \mathrm{V} \overline{x_2} \Lambda \overline{x_1}\,.$$

Table 15.2 – Results of logic operations XOR and XNOR

X_1	X_2	F	
		XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1

The **OR** element **(OR gate).** The output signal *F* of the element is equal to one if at least one of the n-inputs has a signal “1”.

Figure 15.11 shows when signals “1” (- E) are exposed to at least one input (for example, $X_1 = 1$), the corresponding diode (D_1) opens and the output is connected to the input ($F = 1$).

The remaining diodes are closed, i.e. the output signal does not reach the inputs on which $u_{in} = 0$.

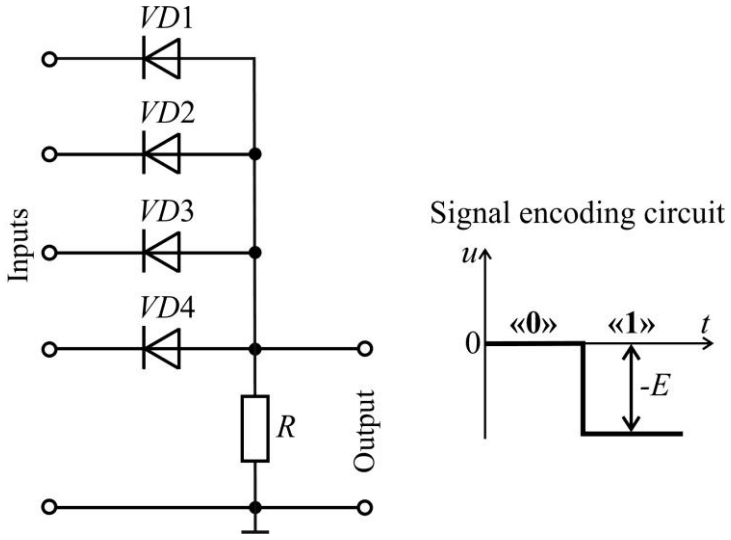


Figure 15.11 – **OR** element

The **AND** element **(AND gate).** Figure 15.12 shows when the signal is “0”, the diodes are open at all inputs (Fig. 15.11), and a current is generated in them and in the resistor *R*, which is generated by the source *E* and closed through the signal source. Since the resistance of the resistor $R >> R_{fr}$, then all outputs signals are “0”.

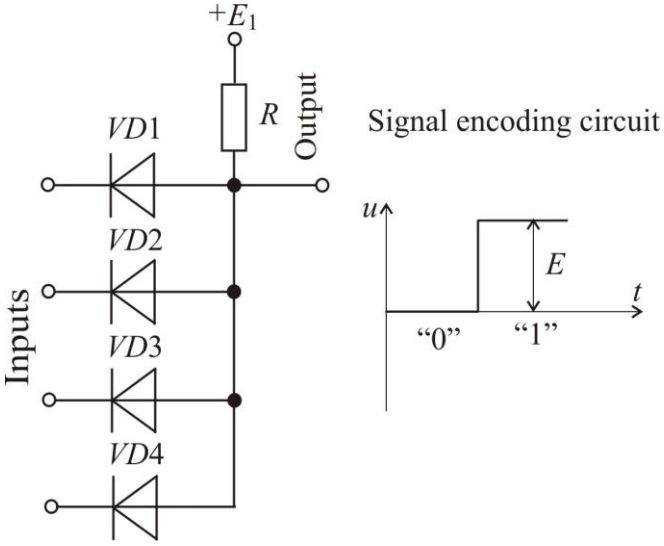


Figure 15.12 – **AND** element

If the voltage at one of the inputs corresponds to a logical “1” ($E > E_1$), then the corresponding diode is closed, but the remaining diodes are open and the signal is still “0” at the output.

The signal “1” at the output will be only when the signal “1” will act on all inputs. In this case, all diodes will be closed, the current through the resistor will be zero and $u_{out} = E_{col}$.

The **NOT** element **(NOT gate)**.

A transistor switch with inverting properties is usually NOT used as an element (Fig. 15.13). In the initial state, the transistor is locked, because the base potential is

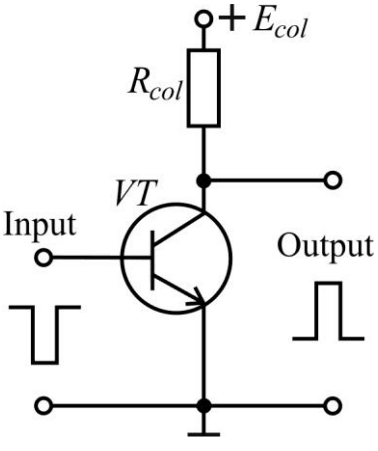


Figure 15.13 – **NOT** element

0. The output voltage corresponds to a logical “1” ($u_{out} = E_{col}$).

When a high (positive) voltage is applied to the base of the transistor, the transistor is unlocked and a low voltage is set at the output – logical “0”.

15.3.7. Triggers, structure and classification of triggers. A trigger (from the English “trigger”) is a device that has two states of stable equilibrium and the property of jumping from one state to another under the influence of an external control signal. Each of these states can be stored for any length of time.

Output voltage drops or trigger steady states can be taken as logic “0” and “1”. In this case, the trigger can be used as a memory device that stores one digit of the number presented in binary code.

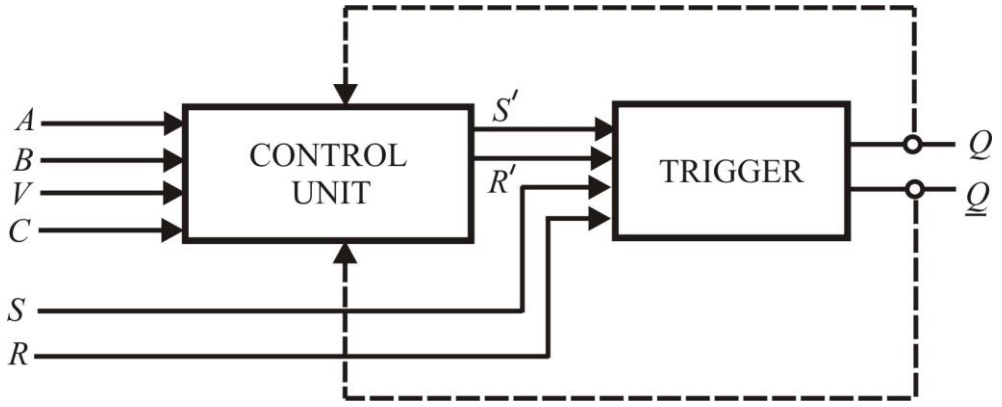


Figure 15.14 – Structural diagram of the trigger system:*A*, *B* – informational (logical) inputs; *V* – preparatory input; *C* – clock (synchronizing) input; *S′* and *R′* are internal inputs; *S* and *R* are external inputs; *Q* and $\overline{Q}$ – external outputs

Triggers are divided into static and dynamic. Triggers in which each state is characterized by an unchanged level (potential) of the output voltage are called static. Static triggers are also called potential triggers. In dynamic triggers, one of the states (usually single) is characterized by the presence of a continuous sequence of pulses of a certain frequency at the output, and the other (zero) by the absence of pulses.

Static triggers, which are implemented on a two-stage amplifier with positive feedback of the galvanic type, have become the most widespread. Each amplifier creates one trigger arm. If both arms have symmetry according to the circuitry and the parameters of the elements included in them, then such a trigger is called symmetrical. If there is no symmetry, then the trigger is called asymmetric.

The structural diagram of the trigger with the control device is shown in Fig. 15.14. Input signals *A, B, V, C, S, R,* depending on the role they play, are divided into informative (logical), preparatory (permitting) and executing (command). The trigger inputs to which these signals are applied are respectively named: informational (logical), presetting (preparatory) and clock (synchronizing). Preset and clock inputs may not be available, and information inputs are present in each trigger. On the diagrams, the trigger inputs are marked in accordance with Table 15.3.

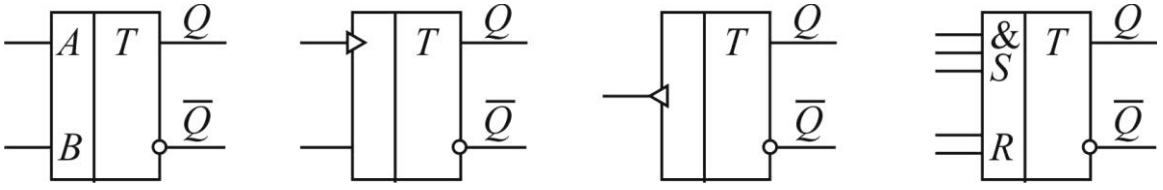
Table 15.3 – Functional assignment of the trigger inputs

Designation	Appointment
S	Input for separate setting of the trigger to the state “1”
R	Input for separate setting of the trigger to the “0” state
J	Input for setting the JK trigger to the “1” state
K	Input for setting the JK-trigger to the “0” state
T	The counting input of the trigger
D	Input for setting the trigger to the “0” or “1” state and control inputs
V	Preparatory input for permission to receive information and preparatory input for receiving information
C	Synchronization input

According to the names of the information inputs, the following are distinguished: *RS*-trigger; *D*-trigger; *JK*-trigger, etc. Depending on the functional diagram of the controlling device, triggers are divided into asynchronous and synchronous.

Asynchronous triggers have only informational (logical) inputs, and information is recorded in them at the time of its arrival. In synchronous triggers, recording of information received at the information inputs is carried out only when an additional command pulse is received at the synchronizing (clock) input. Synchronous triggers can also have asynchronous inputs, which usually serve to set the trigger to the appropriate initial state.

On the diagrams, the trigger is represented by a rectangle divided into two parts (Fig. 15.16). The letter *T* is placed in the right part (main field), and in the left part (additional field) a letter (label) is written near each input, which indicates its functional purpose (Table 15.3).



a *b* *c* *d*

Figure 15.16 – Conditional designations of triggers

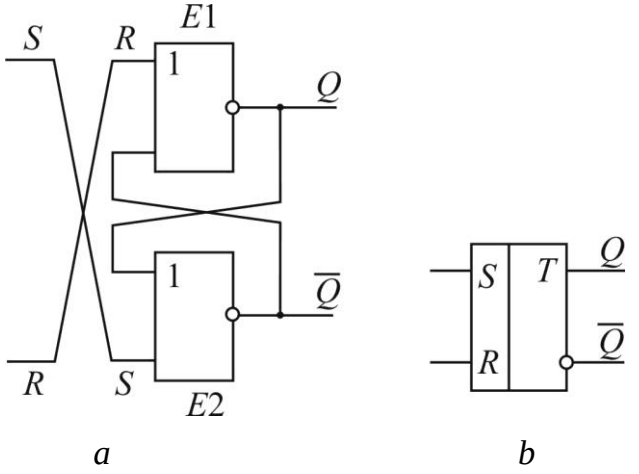
Static direct inputs and outputs are displayed with straight lines, and inverse ones have an indicator in the form of a small circle (Fig.15.16).

Dynamic inputs are indicated by triangles. In direct dynamic inputs, which cause the trigger to "flip" when the signal level changes from "0" to "1", the point of the triangle is directed inward (Fig. 15.6, *b*), and in inverse ones, which cause the trigger to "flip" , when changing the signal level from "1" to "0" - to the outside (Fig. 15.6, *c*).

A trigger can have several information inputs, connected in groups by AND or OR operations.

15.3.8. *RS*-triggers on logical elements. The asynchronous *RS*-trigger on logical elements NOR *E*1 and *E*2 (Fig. 15.17) contains two inputs *R* and S, on which four combinations of logical signals are possible, given in Table 15.4. Where: t^n and t^{n+1} are moments of time before and after the triggering of the trigger; S^n and R^n are signals at the information inputs at time tn, Q^n and Q^{n+1} are signals at the direct output at time tn and t^{n+1}.

The first combination of input signals does not cause the trigger state to change. Indeed, if at the moment of time tn the state of the trigger was characterized by signals $Q^n = 1$, then its output *Q* will have a logical "1" ($Q^{n+1}=1$). At the upper input of element *E*2 there will be a logical "1", at the lower input *S* – a logical "0". As a result, its output $\overline{Q}$ will be logical "0" ($\overline{Q}^{n+1} = 0$).



a *b*

Figure 15.17 – The schematic diagram (*a*) and conventional designation (*b*) of an asynchronous *RS*-trigger on NOR logical elements

Table 15.4 – States of the RS-trigger on NOR elements

t^n		t^{n+1}
S^n	R^n	Q^{n+1}
0	0	Q^n
1	0	1
0	1	0
1	1	X

If $S^n = R^n = 0$ so another equally probable state of the trigger (Q^n=0, $\overline{Q}^n = 1$) can also be stored. This combination of input signals is called a memory mode.

The combination of input signals $S^n = 1,\ R^n = 0$, transfers the trigger to the single state: $Q^{n+1} = 1,\ \overline{Q}^{n+1} = 0$, if it was previously in the zero state (Q^n= 0,

$\overline{Q}^n = 1$). If the trigger was in a single state (Q^n=1, $\overline{Q}^n = 0$), then this combination confirms this state ($Q^{n+1} = 1,\ \overline{Q}^{n+1} = 0$).

The combination of input signals $S^n = 0$, $R^n = 1$ provides the zero state of the trigger ($Q^{n+1} = 0,\ \overline{Q}^{n+1} = 1$), regardless of what it was at the output.

With a combination of input signals $S^n = R^n = 1$, logical “0” ($Q^{n+1} = 0, \overline{Q}^{n+1} = 0$) will appear on both outputs of the trigger. If this is followed by setting a neutral combination of input signals ($S^n = R^n = 0$), then the trigger will assume a single or zero state with equal probability. Therefore, the combination of input signals $S^n = R^n = 1$ for this trigger is called "forbidden" and is marked with the letter X in Table 15.4.

Asynchronous *RS*-triggers are used as memory cells in operational memory devices of a static type. In synchronous *RS*-triggers, the state change occurs, as in asynchronous ones. Therefore, the change of signals at the inputs occurs only in the pauses between synchronizing pulses, to prevent disruption of its operation. The disadvantage of *RS*-triggers is the appearance of undefined states during the formation of forbidden combinations of input signals.

15.3.9. *D*-triggers on logical elements. *D*-triggers (from the English «delay») have one information input *D* and are asynchronous or synchronous. Synchronous *D*-triggers were most widely used (Fig. 15.18).

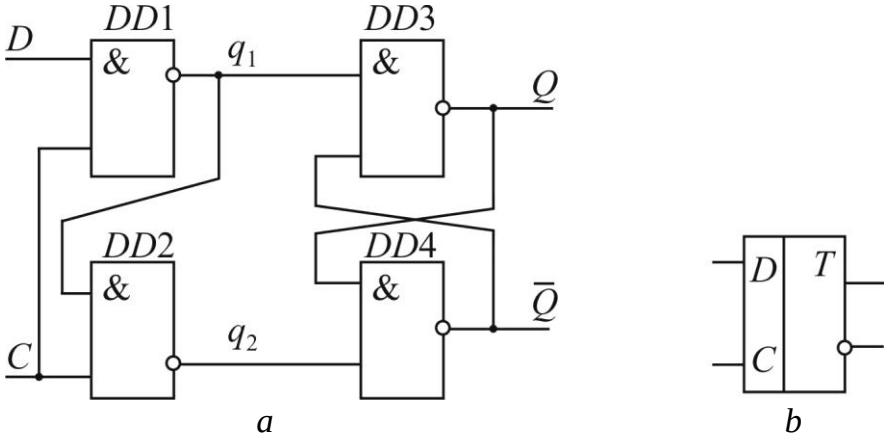


Figure 15.18 – The schematic diagram (*a*) and conventional designation (*b*) of the *D*-trigger on NAND logical elements

Logical elements *DD*1 and *DD*2 form a control circuit. In the absence of a synchronizing pulse (*C* = 0), the logic elements *DD*1 and *DD*2 are closed $q_1 = q_2 = 1$, and the output of the trigger maintains a stable state $Q^n = 1$ or $Q^n = 0$. At the same time, the information at input *D* does not change the state of logical elements *DD*1 and *DD*2 and therefore does not affect the state of the memory cell.

If with the arrival of the synchronizing pulse $C = 1$ there is no signal at the information input D, i.e. $D^n = 0$, then the logic element $DD1$ is closed and $q_1 = 1$. Logical "1" ($C = 1$, $q_1 = 1$) will be applied to both inputs of element $DD2$, it will open ($q_2 = 0$), which will lead to blocking of logical element $DD4$ and unlocking of $DD3$. As a result, a zero state will be established at the output of the memory cell ($Q^{n+1} = 0$, $\overline{Q}^{n+1} = 1$).

If, during the action of the synchronizing pulse $C = 1$, a logical "1" ($D = 1$) is applied to the input D, then the logical element $DD1$ is opened, a logical "0" ($q_1 = 0$) is formed at its output, and the logical element $DD2$ will be closed and $q_2 = 1$. Under the influence of the intermediate signal $q_1 = 0$, the logic element $DD3$ is locked ($Q^{n+1} = 1$), and the element $DD4$ is unlocked, since the signals act $q_2 = 1$ and $Q^{n+1} = 1$.

Thus, the signal at the output Q of the D-trigger takes the same value that is at the information input D during the action of the synchronizing pulse. This value is stored in the trigger until the arrival of the next synchronizing pulse, because in the pauses between synchronizing pulses, a neutral combination of signals acts on the inputs of the memory cell. In the D-trigger, a delay is made for one cycle of the signal that enters the information input D. Therefore, the D-trigger is called a delay trigger.

15.3.10. *JK*-triggers on logical elements. The schematic diagram and designation of the *JK*-trigger is shown in Fig. 15.19.

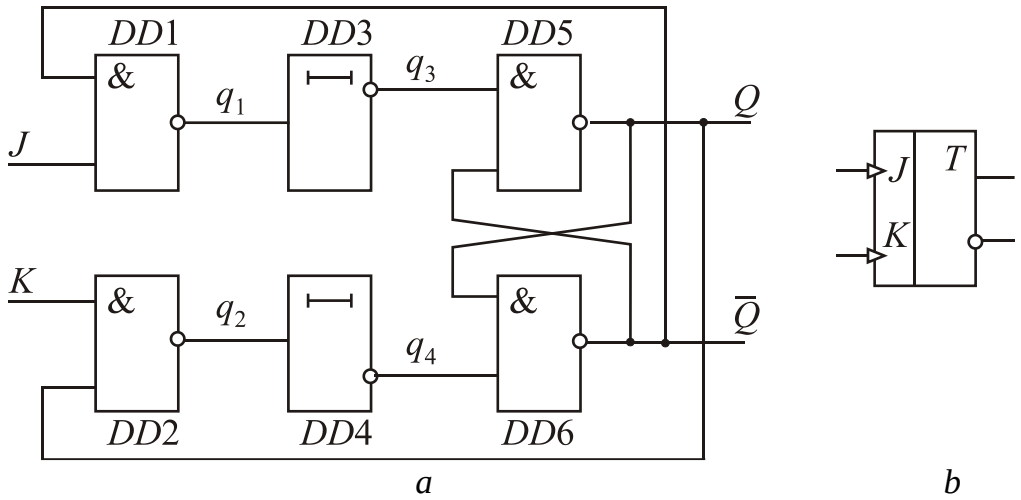


Figure 15.19 – The schematic diagram (*a*) and conventional designation (*b*) of an asynchronous *JK*-trigger

The *JK*-trigger functions in the same way as the *RS*-trigger, with the only difference that it does not have a forbidden combination of input signals. Input J performs the role of input S, and input K is the role of input R. When the input

combination $J^n = K^n = 1$ is equivalent to the forbidden combination for the *RS*-trigger $S^n = R^n = 1$, the state of the *JK*-trigger changes to the opposite.

Logical elements *DD*5 and *DD*6 have a memory cell, which is an *RS*-trigger. Elements *DD*1 and *DD*2 form a control circuit, and elements *DD*3 and *DD*4 delay the signals that enter the memory cell inputs. A feature of the *JK*-trigger is the presence of feedback loops from the outputs to the inputs. Therefore, its state depends not only on the input signals *J* and *K*, but also on the signals Q^n і $\overline{Q}^n$ at the outputs Q and $\overline{Q}$. If $J^n = K^n = 0$, then independent of the signals Q^n and $\overline{Q}^n$ and at the outputs of logical elements *DD*1 and *DD*2 there will be a neutral combination $q_1 = q_2 = 1$ that stores information $q_2 = 1$ in the memory cell.

When $Q^n = 1$ and $\overline{Q}^n = 0$ $J^n = 1$ and $K^n = 0$ and will remain an intermediate signal, and the value of the signal depends on the state of the memory cell. If $Q^n = 1$ and $\overline{Q}^n = 0$, then at the input of element *DD*1 there will be signals $J^n = 1$, $\overline{Q}^n = 0$ and $q_1 = q_3 = 1$. The state of the memory cell will not change. If $Q^n = 0$ and $\overline{Q}^n = 1$, then $q_1 = q_3 = 0$, a signal $Q^{n+1} = 1$ is generated at the output of element *DD*5, and a signal $\overline{Q}^{n+1} = 0$ is generated at the output of logic element *DD*6. Similarly, at $K^n = 1$ and $J^n = 0$, a logical "0" is written into the memory cell, if it was in a logical "1" state, or its zero state is confirmed.

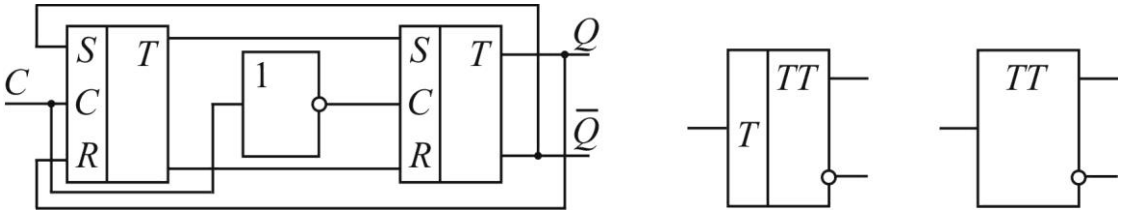
Let now $J^n = K^n = 1$ and $Q^n = 1$, and $\overline{Q}^n = 0$. This will cause a set $q_2 = q_4 = 0$, causing the state of element *DD*6 to change to $\overline{Q}^{n+1} = 1$ and the state of element *DD*5 to change to value $Q^{n+1} = 0$. When $J^n = K^n = 1$ and $Q^n = 0$, $\overline{Q}^n = 1$, there will be $q_1 = q_3 = 0$, as a result of which a signal $Q^{n+1} = 1$ appears at the output of the logical element *DD*5, and $\overline{Q}^{n+1} = 0$ at the output of the element *DD*6. Thus, no matter what state the *JK*-trigger was in, when the input signals $J^n = K^n = 1$ are combined, it is overturned – the state is changed to the opposite.

Delay elements *DD*3 and *DD*4 serve to delay the time of feedback signals from the trigger outputs to the inputs of logic elements *DD*1 and *DD*2. These signals Q^{n+1} and $\overline{Q}^{n+1}$ enter the elements *DD*1 and *DD*2 after the end of the input signals J^n and K^n, that is, when $J^{n+1} = K^{n+1} = 0$. The absence of delay elements would cause the trigger to trigger multiple times. Signals *J* and *K* must be short-lived, which is achieved by controlling the operation of logic elements *DD*1 and *DD*2 along the edge or edge of the pulses. Thus, the *JK*-trigger uses dynamic control of information recording, which is emphasized in its conditional image (Fig. 15.19, *b*). The states of the *JK*-trigger at different values of the input signals are given in Table 15.5.

Table 15.5 – *JK*-trigger states

t^n		t^{n+1}
J^n	K^n	Q^{n+1}
0	0	Q^n
1	0	1
0	1	0
1	1	$\overline{Q}^n$

15.3.11. ***T*-triggers on logical elements.** The *T*-trigger (from the English "toggle" means to turn over) is a trigger with a counting input (or a counting start). It changes its state to the opposite when each trigger pulse is applied to the *T* input. *T*-triggers are easily derived from *RS*-, *JK*-, or *D*-triggers. In Fig. 15.20, and the transformation of a two-stage *RS*-trigger into a *T*-trigger is shown.

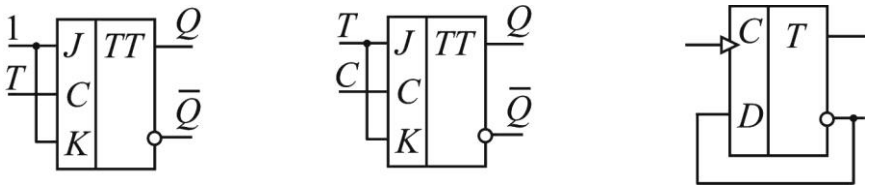


a *b* *c*

Figure 15.20 – The schematic diagram (*a*) and conventional designation (*b*), *T*-trigger made on synchronous *RS*-triggers *c*

In those clocks when $S^n = \overline{Q}^n = 1$, while $R^n = Q^n = 0$ the synchronizing pulse $C = 1$ sets the first trigger to a single state. This state is overwritten in the second trigger after the termination of the synchronizing pulse. It goes to the second trigger using logic elements NOT and NAND. Signals $Q^{n+1} = 1$ and $\overline{Q}^{n+1} = 0$ are generated at the input of the *T*-trigger. When the next synchronizing pulse is applied, the first trigger is set to the zero state by the signal $R^{n+1} = Q^{n+1} = 1$, which is written into the second trigger after the synchronizing pulse ends: $Q^{n+2} = 0$, $\overline{Q}^{n+2} = 1$.

In Fig. 15.21 shows the conversion of a *JK*-trigger into asynchronous (*a*) and synchronous (*b*) *T*-triggers, as well as the conversion of a *D*-trigger with dynamic or two-stage recording control into a *T*-trigger.



a *b* *c*

Figure 15.21 – Conventional designations of *T*-triggers obtained from *JK*-triggers (*a*), (*b*) and *D*-trigger with dynamic control (*c*)

Asynchronous and synchronous *T*-triggers are used in counters and pulse repetition rate dividers.

15.4. Formulation of the problem. Work performance procedure

15.4.1. Draw correspondence tables for the following logical elements: OR; AND; NO; NOR; NAND; INHIBIT, XOR; XNOR.

15.4.2. Connect the "LOGIC" laboratory bench (see Fig. 15.1, 15.22) to the power supply using an adapter. Check the presence of voltage + 5 V using the built-in Voltage Output voltmeter.

15.4.3. On the Fix switching field next to button “1” (upper left corner of the bench) use the jumper to select, for example, the second line on the X switching field (field of a direct, i.e. non-inverted signal). To check the correctness of the use of jumpers, the schematic diagram of the experiment is shown in Fig. 15.22.

After that, when button “1” is pressed, a high-level signal will be sent to the second line of all logic elements. For this, it is necessary to install jumpers on the second line at all x_1 inputs of the test bench elements. To send a signal to the x_2 input of all logical elements, we will use button “2” and the third line, with the exception of modeling the INHIBIT logical element, where the fourth line is used at the x_2 input, see Fig. 15.22.

15.4.4. When button “1” or button “2” is pressed on the switching fields of the corresponding logical elements, the LED corresponding to the logical unit at the input lights up red, and the green LED corresponds to the logical unit at the output of the logical element. A logical zero is obtained by pressing the button a second time or by pulling the jumper from the desired input of the logical element. The logical NOT element is modeled on the OR element, in which the signal is applied to only one of the inputs, for example, input x_1.

In a similar way, we examine all the logical elements sequentially. At the same time, it is necessary to check the result obtained on the bench with the correspondence table of each logical element.

When examining logical elements NAND, NOR, XNOR, NOT, you should choose the inverse output of the logical element – item 2 in Fig. 15.1.

In addition, attention should be paid to the nuances of modeling the logical element of the INHIBIT. It is implemented on logic element AND. Input signals will be monitored on two LEDs near buttons “1” and “3” in the upper left part of the bench. The signal that lights up on the LED near the second input of the AND logic element is already an inverted signal (!). To simulate the INHIBIT logic function, we close the second line on the first switching field near button 1, and on the inverse switching field (field $\overline{X}$) near button “3”, we close the fourth line. Accordingly, we also close the fourth line on one of the inputs of the INHIBIT logic element.

15.4.5. Collect asynchronous *RS*-trigger circuit accepted for research in turn. In Fig. 15.24 shows the circuit of such triggers on the bench: *a*) *RS*-trigger assembled on

NOR logical elements; *b*) *RS*-trigger assembled on logic elements NAND; *c*) *RS*-trigger in the form of one element with the necessary jumpers.

15.4.6. To simulate the signals at the *R* and *S* inputs, we will use buttons 1 and 2 in the upper left part of the bench. Pressing the button causes the red LED next to it to light up, that is, a logic unit is applied to the corresponding input of the trigger. On the switching field, near buttons “1” and “2”, close, for example, the third and second lines, respectively. By setting jumpers on the inverse field, inverse control can be performed.

15.4.7. During the execution of the work, it is necessary to fill in the table of states of the investigated trigger and then check it with the correct table of these states. Attention should be paid to those states in which input information is received and stored or stored information is erased.

15.4.8. Similarly, assemble the circuits of synchronous triggers. In Fig. 15.24 shows the circuit of these triggers on the bench: *a*) *D*-trigger; *b*) *JK*-trigger. Applying informational and control signals to their inputs, make an experimental check of the functioning of the triggers in the sequence specified by the tutor.

15.4.9. In the report, present diagrams and conventional designations of the investigated triggers and state tables illustrating their operation.

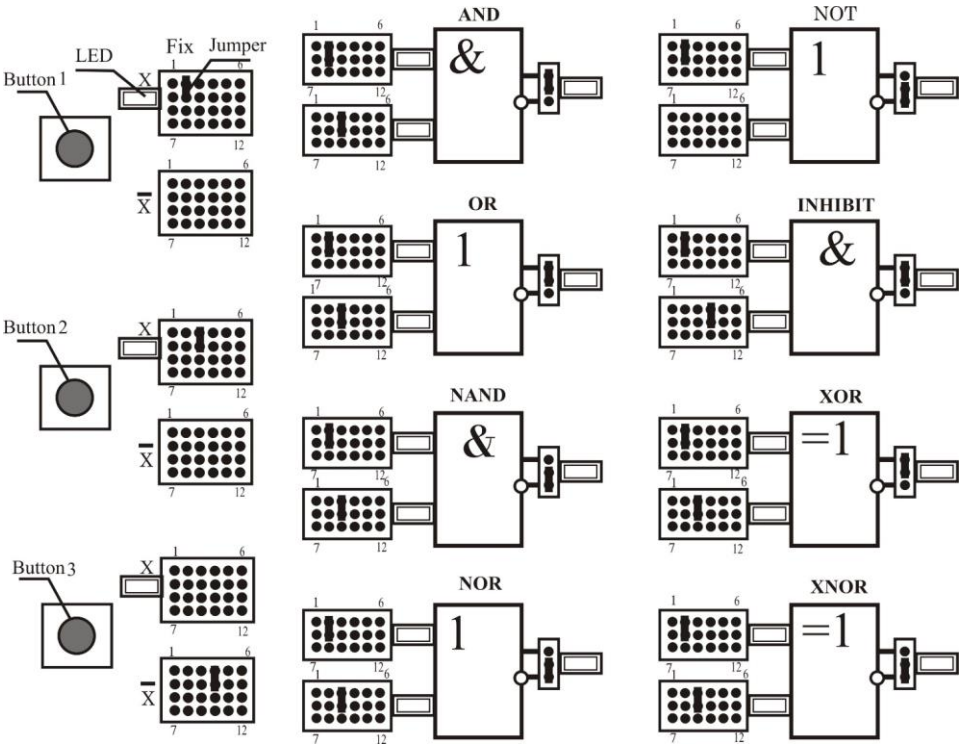


Figure 15.22 – Logical elements with switching fields and jumpers on the "LOGIC" bench

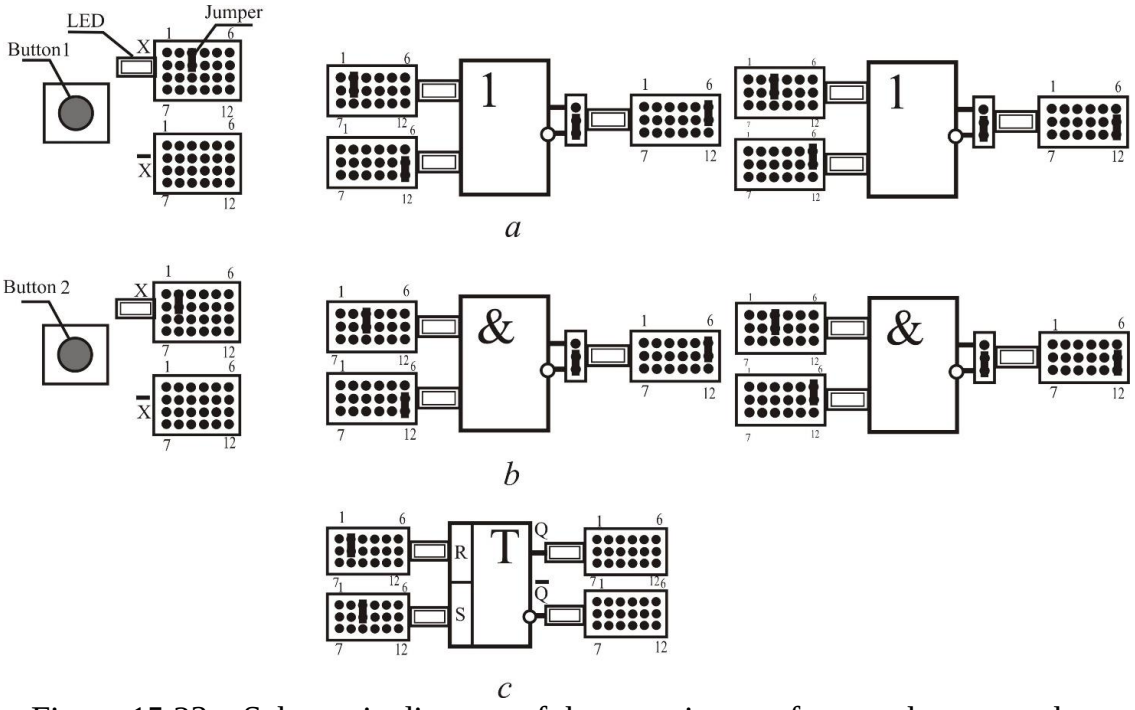


Figure 15.23 – Schematic diagram of the experiment of research an asynchronous *RS*-trigger on the TRIGGER bench:
a - on NOR elements; *b* – on NAND elements; *c* - on one element

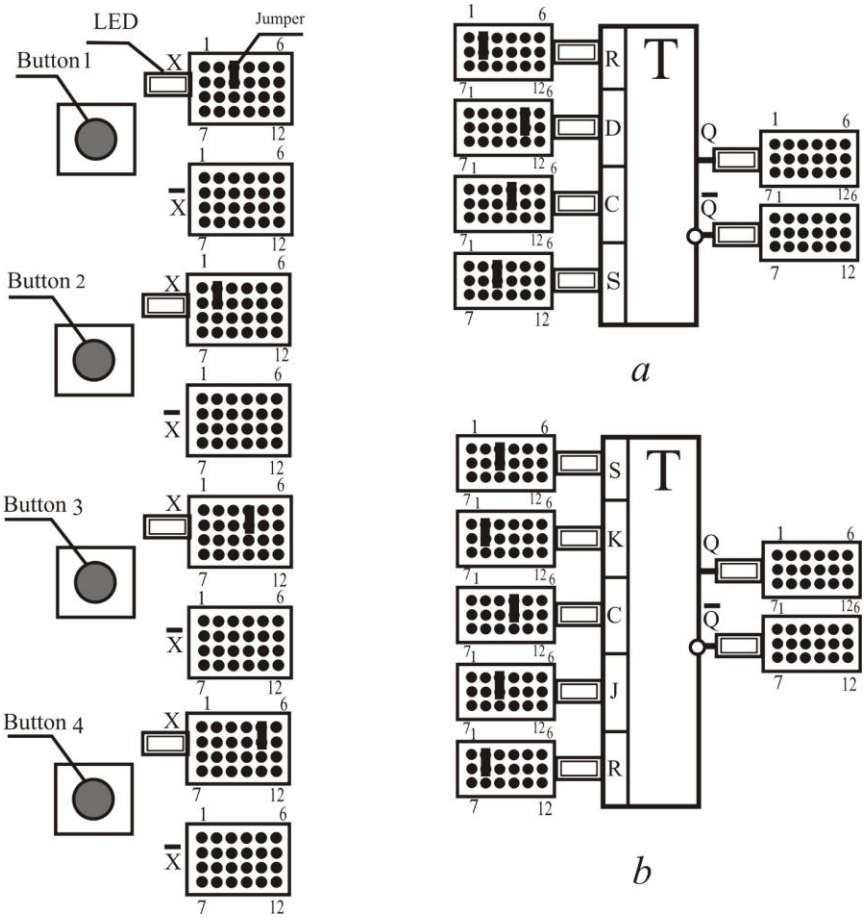


Figure 15. 24 – Schematic diagram of the experiment for the study of synchronous triggers on the TRIGGER bench: *a* - *D*-trigger; *b* – *JK*-trigger

Control Questions

1. State and explain basic logical operations.

2. Give the conditional designations of logical elements that implement the logic operations OR, AND, NOT, NOR, NAND, INHIBIT, XOR and XNOR.

3. List the results of logical operations OR, AND, NOT, NOR, NAND, INHIBIT, XOR and XNOR.

4. Explain what is a trigger? What are static and dynamic triggers?

5. Give the structure and classification of triggers. Draw the structural diagram of the trigger system.

6. Draw the diagram and conventional notation of an asynchronous *RS*-trigger on NOR logical elements. Explain how this trigger works.

7. Draw the diagram and conventional notation of an asynchronous *RS*-trigger on logic elements NAND. Explain how this trigger works.

8. Draw the diagram and conventional notation of the synchronous *RS*-trigger on logical elements NAND. Explain how this trigger works.

9. Draw the schematic diagram and conventional notation of the synchronous *RS*-trigger on logical elements NOR. Explain how this trigger works.

10. Draw the diagram and conventional notation of the *D*-trigger on logical elements NAND. Explain how this trigger works.

11. Draw the diagram and conventional designation of an asynchronous *JK*-trigger. Explain how this trigger works.

12. Draw the schematic diagram and notation of the T-trigger made on synchronous *RS*-triggers. Explain how this trigger works.

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FOR NOTES

Навчальне видання

Укладачі:
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«Електротехніка, електроніка та мікропроцесорна техніка»
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